Final Year Design Project as a Complex Engineering Problem

It is to certify here that the final year design project (FYDP) entitled,

"Design and Implementation of FPGA based Coupled Inductor Diode Assisted Boost Inverter"

is categorized as a complex engineering problem (CEP) based on the preamble (in-depth engineering knowledge) and involvement of the following attributes.

1. Depth of knowledge required
2. Depth of analysis required
3. Range of conflicting requirements
4. Consequences
5. Interdependence

The above listed attributes are thoroughly assessed after conducting meeting on 3rd November 2022, with the following final year students, who proposed the idea of the titled FYDP.

1. Name: Abdul Rehman
   Reg No: ECI-IT-19-073
2. Name: Shahzaib Sanwal
   Reg No: ECI-IT-19-031
3. Name: Syed Khurram s
   Reg No: ECI-IT-19-030
4. Name: Jawad Hussain
   Reg No: ECI-IT-19-032

This project is going to be conducted in fall semester 2022 and spring semester 2023. Further, it is submitted that the proposed idea is worthy, and the required efforts are up to the level of a final year design project.

FYDP Advisor
Engr. Kamran Khan

1.7 Complex Engineering Problem

This project satisfies the attributes of the complex engineering problem, in the given context, this section presents the justification that how the presented work addresses different attributes of the complex engineering problem. The details are presented in Table Error***! No text of specified style in document.***..

Table **Error! No text of specified style in document.**.1 CEP Attributes Mapping

Sr. No	**Attribute**	**Justification**
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3	Depth of analysis required	Analysis of various boosting techniques like z-source, T-source, pi-source and coupled inductor boost inverters for the optimal response.
4	Consequences	Green energy and positive environmental effect highlight projects success
5	Interdependence	Inductor size, charging time of coupled inductor and shoot through currents are interdependent

Sustainable Development Goals

This section presents a brief overview of all the SDGs and mainly justifies the contribution of the project to the sustainable development goals (SDGs). Detailed justification of the mentioned points is presented in Table Error***! No text of specified style in document.***.

Table **Error! No text of specified style in document.**.2 SGD Table of the Project

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1	No poverty	Yes	Cheap and efficient Photovoltaic integration with the power grid
2	Zero hunger	No	Not applicable
3	Good health/wellbeing	Yes	Shifting to Renewables and Electrical Vehicles will cause lower pollution
4	Quality education	No	Not applicable
5	Gender equality	No	Not applicable
6	Clean water and sanitation	No	Not applicable
7	Affordable and clean energy	Yes	Cleaner energy through renewable sources
8	Decent work and economic Growth	yes	The project can be used in renewable energy systems, electrical drives and Electrical vehicles.
9	Industry, innovation and Infrastructure	Yes	Project contributes to the advancements in the automotive industry and renewable energy sector
10	Reduced Inequalities	No	Not applicable
11	Sustainable Cities and Communities	Yes	Renewable energy sources contribute towards lower pollution thus sustainable cities and communities
12	Responsible consumption and	Yes	The project reduces dependance of

	Production		fossil fuels
13	Climate action	Yes	Low carbon emissions with renewables
14	Life below water	No	Not applicable
15	Life on land	No	Not applicable
16	Peace, Justice and strong Institutions	No	Not applicable
17	Partnerships for the goals	No	Not applicable

ABSTARCT

The adoption of renewable energy sources like solar and wind energy has raised the demand in recent years for efficient and dependable electricity. This has led to the development of new topologies and control strategies for power converters that can operate in different operating conditions. This project comprises of a FPGA based single stage diode assisted three phase SPWM boost inverter with distinct DC voltage source and a conventional three output legs (one leg for each phase), which is efficient for low DC power sources and utilize coupled-inductor to boost input DC link voltages to get the high AC output power. The hardware results show that the performance of the FPGA-based SPWM three-phase boost inverter achieves high average DC gain, excellent DC-AC coupling, low voltage stress on switches and low distortion in output AC voltages. The FPGA is used to generate the SPWM signal for the control of inverter switches. A new model of the three-phase boost inverter has been developed and tested by implementation control scheme on FPGA Spartan-3E Starter Board. According to experimental, findings, the proposed inverter topology operates at a maximum power of 1kW while maintaining an efficiency above than 80%. Total harmonic distortion (THD) of the output voltage is less than 30%, and the output voltage control accuracy is $\pm$5%.

Final Year Design Project as a Complex Engineering Problem

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Design and Implementing of FPGA based Coupled Inductor Diode Assisted Three Phase Boost Inverter

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FYDP Advisor	FYDP Co-Advisor
Engr. Kamran	**Engr. Talha Riaz**

ACKNOWLEDGMENT

Acknowledgment is due to **Faculty of Engineering Science and Technology** for support of this project highly appreciated achievement for us at the undergraduate level.

We wish to express our appreciation to the **Engr. Kamran khan** who served as our supervisor. We would like to express our heartiest gratitude for their keen guidance, sincere help, and friendly manner which inspires us to do well in the project and makes it a reality.

We thank **Engr. M Talha Riaz** who served as our co-supervisor. We would like to express our heartiest gratitude for their keen guidance and assistance in keeping our progress on schedule.

LIST OF CONTENTS

LIST OF FIGURE

LIST OF TABLE

ABBREVATIONS

DC	Direct Current
AC	Alternating Current
THD	Total Harmonic Distortion
FPGA	Field Programming Gate Array
PWM	Plus Width Modulation
SPWM	Sinusoidal Plus Width Modulation
CL-DABI	Couple Inductor Diode Assisted Boost Inverter
IGBT	Insulated Gate Drive Bipolar Transistor
VSI	Voltage Source Inverter
CSI	Current Source Inverter
CMLI	Cascaded Multilevel Inverter
DCMLI	Diode Clamped Multilevel Inverter
FCMLI	Flying Capacitor Multilevel Inverter
ZSI	Z-source inverter
UPS	Uninterruptible Power Supply
ASIC	Application Specific Integrated Circuit
SDG	Sustainable Development Goals

Chapter 1

Introduction

The need for effective and reliable power inverters has grown in recent years due to the increasing use of renewable energy sources such as solar and wind. Due to the widespread usage of sources that generate DC like fuel cells, solar panels, and wind turbines, inverters have been a hot topic in recent years. Power backup systems must include inverters as a component. Applications going from power sensitive applications to universally useful UPs for family utilize all require power backup. Uninterruptible power supply is very essential for defense purpose equipment's like radar and anti-missile control systems. Uninterruptible power supply is not possible without inverters. They're also used in industrial applications like motor variable frequency drives. Many industries need essential AC power supply for sensitive process and control systems like oil refinery and nuclear production plants. Changing the voltage level of AC is necessary in certain applications. High-frequency DC-DC converters are now considered more viable to convert voltage levels in the DC domain as a result of the advancement of power electronic devices. In such systems, AC electricity is transformed to DC and then back to AC using inverters after passing through a DC-DC converter stage. As a result, inverters are becoming an increasingly important component of systems whose output dictates the overall system's output power quality.

1.1 Motivation

Due to its advantages for the environment, dependency on fossil fuels, renewable energy sources like solar and wind power have gained popularity in recent years. Mostly renewable energy sources produce DC power, therefore inverters become essential for convert DC power into AC Power for domestic and industrial use.

1.1.1 Enhanced Energy Conversion Efficiency

The proposed FPGA-based three phase boost inverter is efficiently modulating the output voltage through SPWM technique, this inverter can ensure that the maximum power generated by renewable energy sources is effectively converted and injected into the grid. This enhanced energy conversion efficiency can lead to reduced energy losses, increased utilization of renewable resources, and ultimately, a greener and more sustainable energy ecosystem.

1.1.2 High Gain Voltage Conversion

The incorporation of a boost stage in the inverter topology allows for voltage step-up, enabling the inverter to match the generated renewable energy voltage levels to the grid requirements. When dealing with low-voltage renewable energy systems, the high gain provided by the three-phase boost inverter which can reduce the need for additional intermediate voltage conversion stages, reducing complexity and cost.

1.1.3 Robust Grid Integration

The FPGA-based control system for the High Gain Three Phase Inverter allows for precise control of output voltage, frequency, and phase angle. This enables seamless integration with the grid's voltage and frequency levels, contributing to grid stability and reliability.

1.1.4 Real-time Adaptability

The utilization of FPGA technology provides a powerful platform for real-time control and adaptability [2]. FPGAs allow for the implementation of complex control algorithms and modulation techniques, ensuring rapid response to changes in input conditions or grid requirements [2]. This adaptability is essential in managing the variability of renewable energy sources and maintaining consistent power output [2].

1.1.5 Research and Innovation

The design of a FPGA based Three Phase Boost Inverter using FPGA technology is modern technology for research and innovation. Developing control algorithms, optimizing modulation techniques, and engaging the system reliability can contribute to advancements in power electronics systems, FPGA implementation, and renewable energy integration.

1.2 Problem statement

Renewable energy sources are growing rapidly to meet domestic and commercial electricity demands. Wind, solar, hydroelectricity, and other renewable energy sources are reducing and inefficient. Renewable Energy technologies, like hydrogen/hydrocarbon fuel cells, may produce power from chemical processes. Other directly generating electricity resources include fuel cells and solar energy[3]. Mostly renewable energy resources produce lower DC power which is not stable therefore its need to convert into stable AC power for domestic and industrial utilization.

The DC power then be converted into AC power or directly connected to the load.

The slow rate of DC to AC conversion is another issue. The maximum AC output voltage of inverter is measurable. AC output of inverter can be found using equation (1). The maximum RMS voltage will be one-third of the DC link. When $m = 1$. Since most resources produce low DC power, a high boost is required before converting DC power [4].

$$Vac = \frac{mVdc}{2} \qquad (1)$$

$$where: 0 < m < 1 - for\ SPWM$$

Where m is the modulation index, Vac is the AC voltages, & Vdc DC voltages Conventional boost inverters may theoretically offer significant voltage improvements with duty cycles close to one, but this leads to poor dynamic responsiveness. In order to solve challenges like greater gain, improved efficiency, better reliability, and a fewer number of components, which results in lower cost and size [4], single stage boost topologies have been designed.

The implementation of Pulse Width Modulation (PWM) techniques in inverters is essential to achieve high-quality AC waveforms. However, existing PWM-based inverters often suffer from low efficiency, complex control algorithms, and limited flexibility in terms of boosting the output voltage. The purpose of this project is to design, develop, and implement an FPGA-based Three-Phase SPWM (Sinusoidal Pulse Width Modulation) Boost Inverter system that addresses power conversion challenges and meets the growing demand for efficient renewable energy integration.

1.3 Aims & Objectives

We will able to achieve the following objectives by implementation FPGA based three-phase coupled inductor diode-aided boost inverter with high gain.

- Reduce inverter size by replacing multistage boost converter with single stage coupled inductor based inverter.
- Reduce total harmonic distortion (THD).
- Use of FPGA board for efficient control.
- Use of SPWM (sine wave plus width modulation) to avoid shoot through switching.
- Improve boost inverter efficiency.
- Reduce Voltage spikes.

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Chapter 2

Literature Review

Inverter is an important device of electrical power used to convert direct current (DC) to alternating current (AC) and also in power applications, uninterruptible power supply (UPS), solar energy, inverter plays an important role in many applications such as now days cannot meet our needs with energy produced from non-renewable materials. Therefore, we meet our energy needs using renewable energy, there is usually renewable energy resources have not stable DC output, so we need to have a boost inverter for domestic and industrial use. Inverters play an important role in integrating renewable energy into the grid. Renewable energy sources such as solar panels and wind turbines produce direct current (DC) electricity, which is used after converting into the alternating current (AC). Inverters ensure that electricity produced from renewable energy sources is compatible with existing systems, ensuring its distribution and efficient use. They can also be synchronized with the mains frequency and voltage, making the power stable and reliable. Inverters are important components that facilitate the integration of renewable energy into modern electrical systems.

2.1 Inverter Topologies and Their Drawbacks

Three-phase inverter topologies offer various trade-offs in terms of output waveform quality, efficiency, complexity, and cost. While each topology has its advantages, such as reduced harmonics or improved voltage stress management, they also come with their own drawbacks. These limitations include increased complexity, higher component count, control challenges, and potential reliability issues. Researchers and engineers continue to explore ways to mitigate these drawbacks and optimize the performance of three-phase inverters in various applications.

2.1.1 Voltage Source Inverter (VSI)

Voltage Source Inverters are widely used in various applications due to their simplicity and ease of control. However, their key drawbacks include voltage distortion due to the presence of harmonics in the output waveform, and their inability to regulate reactive power, which can impact the quality of power supplied to the grid.

A simple solution may be another voltage source inverter (VSI). Here, the voltage originating from the inverter is raised using a filter and a step-up transformer.

However, there are a number of drawbacks to this transformer-based system, including its high cost, large volume, bulky design, and loud noise [5]. To satisfy the load requirement, a dc-dc converter fed VSI (for increasing dc voltage) is a common option. However, this design calls for an extra solid-state switch, power diode, inductor, and electrolytic capacitor bank to get the necessary dc link voltage because it is connected to two separate control structures. The configuration of a two-stage power conversion system has a number of disadvantages, such as a larger part count, lower efficiency, and the need for two distinct control techniques [5]. Additionally, VSI needs time delay circuits to prevent shot through when dead band time generation occurs between switches on the same leg. This feature lowers the dependability and quality of the power [5].

2.1.2 Current Source Inverter (CSI)

Current Source Inverters are less common compared to VSIs but find application in certain specialized scenarios. They maintain a constant current output, which can be advantageous in specific applications. However, their main drawback is that they are generally more complex to control and implement, and they can suffer from instability issues at low modulation indices [5]. One significant drawback of CSI is its inherent current control instability at low modulation indices, which can lead to poor dynamic performance and instability in the output current waveform. This instability arises due to the abrupt changes in output current magnitude and phase caused by variations in load and supply voltage [5]. Furthermore, the CSI topology often requires large inductor components for proper operation, leading to increased size, weight, and cost of the overall system. This can be particularly problematic in applications where space and weight constraints are critical, such as in automotive and aerospace systems.

CSI's inability to provide voltage boosting further restricts its use in applications requiring voltage step-up capabilities. It also faces challenges in terms of efficiency, as the constant current output characteristic may lead to higher losses during operation compared to voltage source inverters [5]. These drawbacks have motivated researchers and engineers to explore alternative converter topologies, such as Voltage Source Inverters (VSIs) and Multi-Level Inverters (MLIs), which offer improved control performance, better efficiency, and enhanced voltage handling capabilities. Overall,

while CSI has found applications in specific niches, its limitations hinder its widespread adoption in modern power electronics systems [5].

2.2 Multilevel Inverter Topologies

There are three different topologies for multilevel inverters. Diode clamping multilevel inverters, flying capacitors multilevel inverters, and cascaded H-bridges multilevel inverters. Each one of these can produce output of high-quality and has various benefits, but their structure and disadvantages may make them ideal for specific applications.

2.2.1 Diode-Clamped Multilevel Inverter (DCMLI)

The most widely used multi-level topology is the diode clamp inverter, in which diodes are used as clamping devices to clamp the DC bus voltage to achieve a step in the output voltage [6]. Diode clamping inverters provide multiple voltage levels by connecting each level to a series of capacitors. According to the original invention, the idea can be extended to any level by increasing the number of capacitors. The main advantage of DCMLI If there is enough level the total harmonic distortion (THD) will be very low. This is one of the advantages of diode clamped multilevel inverters [7]. All electronic converters are efficient because they only change at a fundamental frequency. The change process is very simple. The main disadvantage of

DCMLI is that it is very difficult to stabilize the capacitor voltage and many clamping diodes are required for higher level inverters [8].

2.2.2 Flying Capacitor Multilevel Inverter (FCMLI)

Capacitor clamped inverters, also known as flying capacitors, are one of the alternative topologies to diode clamped inverters. Flying capacitor can be connected stepwise to increase or decrease the voltage [9]. Its main advantage is that the required voltage levels can be achieved without the use of transformers. This helps to reduce the cost of the converter and also reduces power loss. Unlike the diode-clamped model, where series capacitor banks share the same voltage, in a capacitor-clamped voltage converter, the capacitors in the two legs are charged at different voltage levels. To combine the phase voltage waveforms, several switches on the two legs are opened to combine the various capacitor voltage levels, with the limitation of the absence of short capacitors and the storage of galvanic continuity of each DC-connected capacitor [10]. The main disadvantage of FCMLI compared to other topologies is the size of the

capacitors required. Capacitors are large and expensive. The initial charge of capacitors is a demanding process. It is difficult to keep track of the voltage levels of all capacitors [10].

2.2.3 Cascaded Multilevel Inverter (CMLI)

A step-down multi-level inverter (CMLI) consists of a series of single-phase full-bridge inverters. After 1997 stepper multilevel inverters became popular. They have been widely used ever since because of their advantages over other types of multilevel inverters. Step-up multilevel inverters combine discrete DC voltages to produce a functional sinusoidal output waveform. In this topology it is a CMLI level. A series H bridge is required in a phase inverter [11]. Each bridge has a separate DC power supply. The concept of multilevel inverter is based on connecting H-bridge inverters in series to obtain a sinusoidal voltage output. A full bridge itself is a three-phase step-up H-bridge multi-level inverter, and each additional module in the stepping expands the inverter to two voltage levels. Each bridge inverter produces three voltages VDC, 0 and −VDC. To distinguish a vCHB level, a multilevel inverter opens one switch in a full-bridge inverter and closes the other. A stepwise H-bridge inverter uses a series of individual H-bridge units to produce multi-level output. They facilitate expansion by providing good waveform quality and modularity [11].

However, the complexity and cost associated with multiple H-bridge cells can be significant, particularly at higher voltage levels. The primary drawback CMLI is there should be isolated DC power supply [12].

2.2.4 Z-source inverter (ZSI)/qZ-Source Inverter

To overcome other problems of the topology, such as operating and supporting capacity at shutdown conditions, many additional inverter topologies have been proposed by arranging the DC input and return impedance networks in different ways. The X-shaped LC impedance network is placed to be supported by the operation of the alternative network in the previous mode [13]. Similar to Z-source inverter (ZSI), this paper proposes various impedance mesh-based inverter topologies such as quasi-ZSI (qZSI), switching ZSI, Switching Amplifier Inverter (SBI) [13], Inductor-ZSI(). L-ZSI), Switched Inductor (SL)-ZSI [14], SL-qZSI [14], Diode powered qZSI, Capacitor powered qZSI and Extended Boost ZSI [15].

These topologies are mostly recommended for improving dc-ac conversion gain, lowering capacitor voltage stresses, or minimizing the number of components. However, all of the aforementioned topologies result in phase and line voltages with a pulse width modulation (PWM) characteristic, which, like VSI, results in voltage and current harmonics. Increasing the inductors and/or capacitors will increase the influence of nonlinearity [16].

2.3 Coupled-Inductor Diode Assisted Boost Inverter

In this topology, the four diode and a coupled inductor is connected in such a way that there is shot through to raise the average DC voltage. Connecting a small value capacitor its improves DC-AC coupling and helps reduce dv/dt. Power switches are under voltage stress during switching operation of inverter. The single-phase boost inverter that the researchers introduced in [17] and employed in the proposed CL-DABI. Contrarily, CL-DABI has the capacity to turn enormous amounts of electricity into improved quality. High gain and improved conversion efficiency are obtained in the suggested inverter while minimizing the usual downsides, such as dv/dt voltage stress, This project presents an FPGA-based, high-gain, three-phase, coupled inductor diode-assisted inverter (CL-DABI) which can reduce all problems of other inverters and fulfil energy demands efficiently. Coupled inductors help achieve good results by choosing the right inductor turns ratio.

Using the pulse width modulation (PWM) concept, it has been shown that low switching and high DC voltages cause voltage stress on the switches of the device. Therefore, sinusoidal PWM is introduced to achieve the maximum efficiency of the three-phase inverter.

Chapter 3

Proposed Methodology

The whole project that is being implemented in this thesis, a FPGA based High Gain Coupled Inductor Diode Assisted Three Phase Boost Inverter. First there is single phase 220V supply that is coming through grid station which is being supplied to transformer, these transformer step down the input then connected to bridge rectifier, which convert the AC supply into DC supply or direct DC renewable energy source can be use. The output of the first bridge rectifier is then supplied to a three-phase inverter which produces the three phase AC output.

The IC gate driver (gate pulse generator) is also connected to FPGA which is basically controlling the switching schemes. The low voltage signal from the IC controller is provide to gate drive circuit which boost control signal voltages for high power switches, like an IGBT or power MOSFET. FPGA is working as gate pulse driver and control switching operation of the three-phase inverter.

3.1 Operation of Proposed Scheme

The schematic diagram of the three-phase CL-DABI is shown in Figure 1. The six switches S1 to S6 in this inverter are connected in figure 1. Three power diodes also connected in power circuit, the power diodes provide a short path for the inductor to charge and ensure unidirectional energy flow to the capacitor, Diode D is connected. Connected inductors that fulfill the inverter's precise gain requirements. LC filter is also used to eliminate three-phase voltage harmonics.

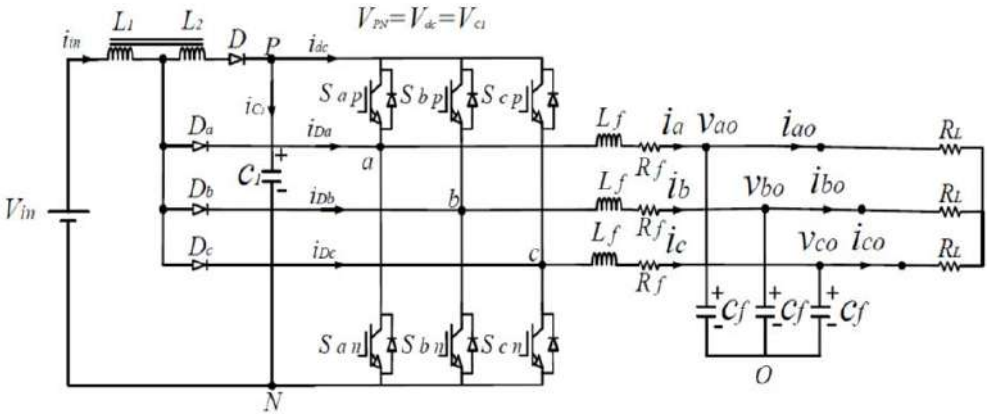

Figure 1: Schematic diagram of combined inductor diode assisted inverter

The possible operation of the switches is discussed below. State I in figure 2 is the first zero crossing state (ie 000) with all voltages below San, Sbn and Scn open and all switches open, upper Switches, Sbp and Scp disabled. The voltage across the load is zero and all three diodes Da to Dc charge the inductor L1 with a current gradient, leading to undervoltage on both legs of each phase. The current is divided equally between the three diodes Da-Dc and the capacitor current ic1 becomes zero.

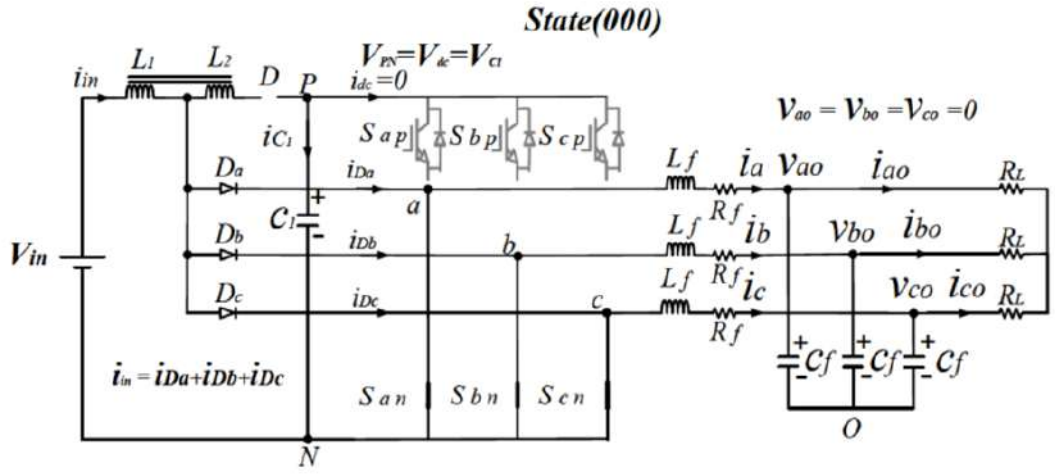

Figure 2: Proposed three-phase inverter state I schematic diagram

Non-zero state transition II in Figure 3 has three paths (ie 001, 010 and 100). The combination of three Si, p (i = a, b, c) changes and two low Si, n changes will do the job of the corresponding diode. The load will be powered from the charging capacitor C1.

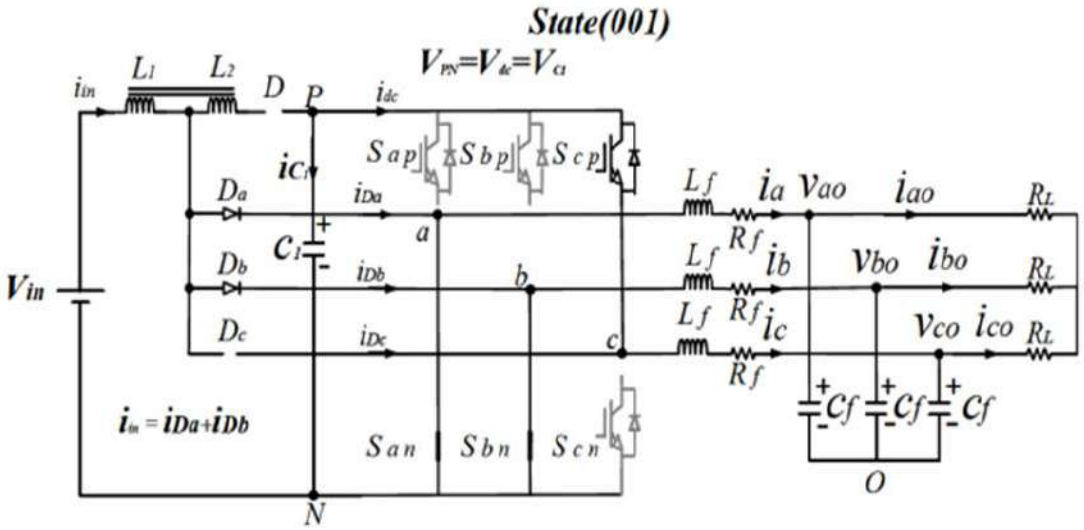

Figure 3: Three-phase inverter Non-Zero Switching state II schematic diagram

Figure 4 shows transition state III, which also has three non-zero states (i.e. 011, 101 and 110). The combination of two upper Si, p and a lower Si, n. At this time, diode D and two of the three Da-Dc will reverse. An additional diode will do, allowing maximum current to flow through it.

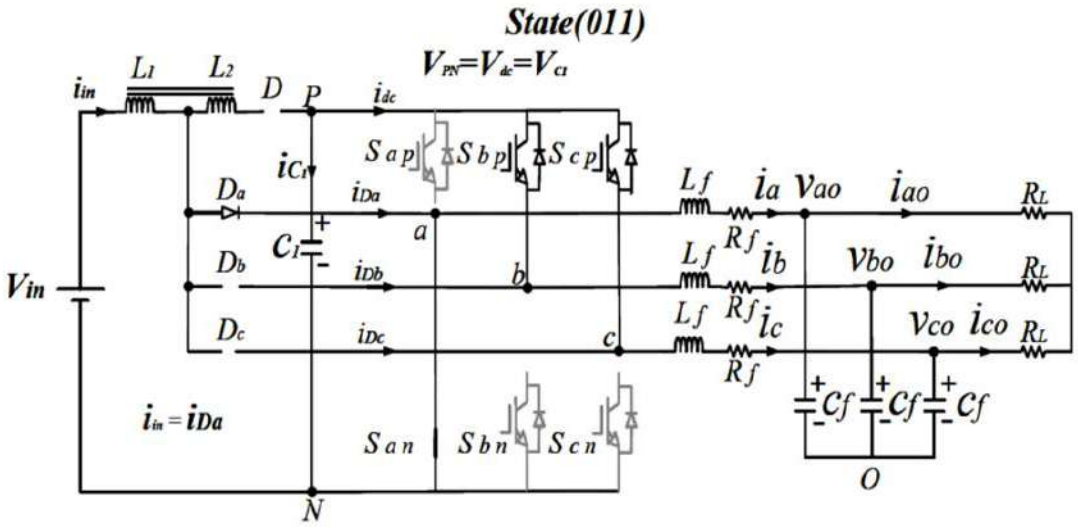

Figure 4: Three-phase inverter Non-Zero Switching state III schematic diagram

In the second zero state (eg 111), in state IV figure 5, all the upper switches Si, p are open, and the lower switches Si, n are all closed. All Da-Dc diodes are reverse polarized because the high capacitor voltage appears on the cathode side. Coupled-inductors L1 and L2 are disconnected from capacitor C1 through diode D. Table 3 shows the status of the device in each case mentioned above.

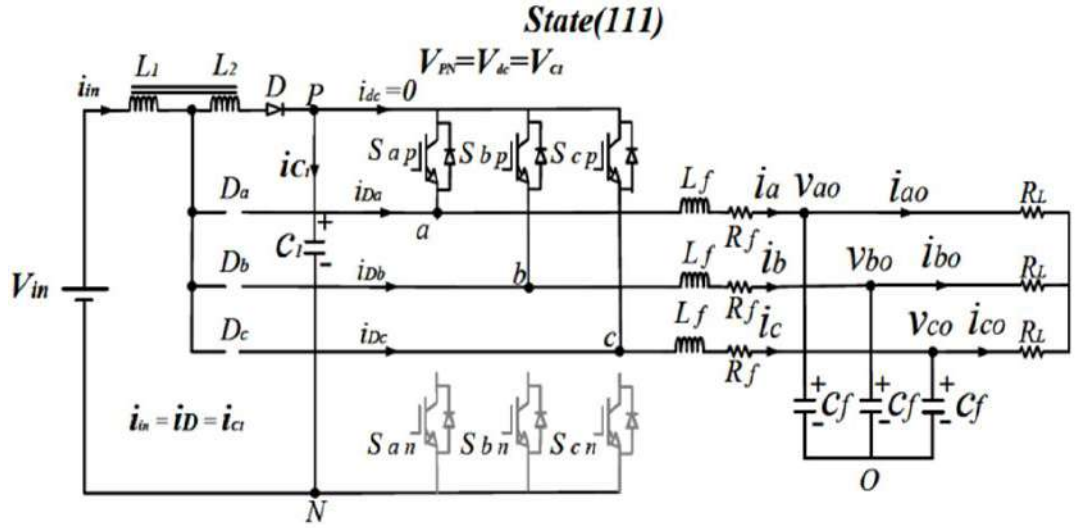

Figure 5: Three-phase inverter Non-Zero Switching state IV

Table 3: switching states

State	I	II			III			IV
Switches	(000)	(001)	(010)	(100)	(011)	(101)	(110)	(111)
D	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
D_a/S_{an}	ON	ON	ON	ON	ON	OFF	OFF	OFF
D_b/S_{bn}	ON	ON	OFF	ON	OFF	ON	OFF	OFF
D_c/S_{cn}	ON	OFF	ON	OFF	OFF	OFF	ON	OFF
S_{ap}	OFF	ON	OFF	ON	OFF	ON	ON	ON
S_{ap}	OFF	OFF	ON	OFF	ON	OFF	ON	ON
S_{ap}	OFF	OFF	OFF	OFF	ON	ON	OFF	ON

3.2 Block Diagram

The block diagram of the proposed Inverter is shown in figure 6.

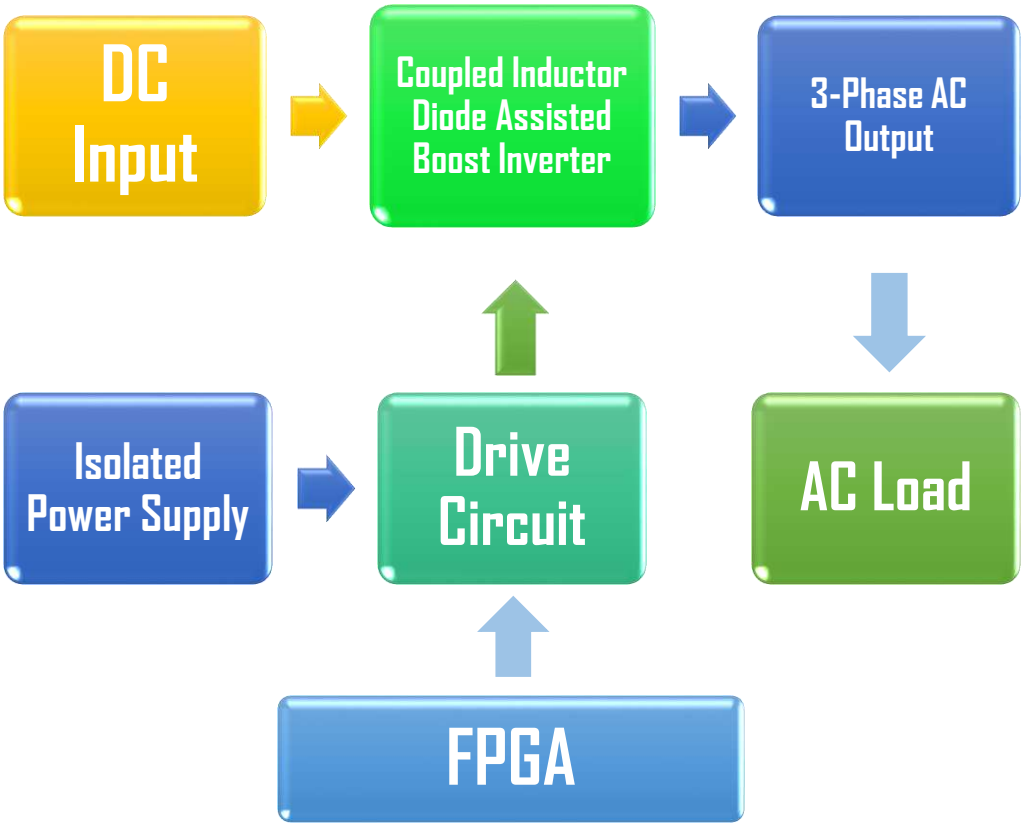

Figure 6: Block Diagram

The operation of proposed inverter is controlled by FPGA which input is boosted by gate drive circuit. Drive circuit is connected with isolated power supply, which is connected with 220V AC. Gate drive circuit is preferred for boosting of control signals in the inverter. Gate drive is most part of this three-phase inverter which isolate the FPGA from high voltages and also boost FPGA output. AC power is stepped down to 15V by using potential transformer of appropriate rating and covert it to DC power by using rectifier. The gate drive Circuit uses this 15 VDC to provide a boosted input low voltage signa;, which used to drive switches of the proposed three phase inverter.

The input DC power will be generated by available any renewable sources which will be fed to FPGA Based Three Phase Boost inverter through coupled Inductor. Proposed inverter will convert input DC power to three phase AC power. Coupled inductor boost the low input DC power into High DC power. Coupled inductor play main rule for boosting DC supply. Three power diodes also connected in power circuit, the power diodes provide a short path for the inductor to charge and ensure unidirectional energy flow to the capacitor

Field Programmable Gate Array (FPGA) generate SPWM and fed it to gate drive circuit which boost the control signal pulses for operate to switches of inverter. Gate driver circuit amplifying the pulses and provide isolations by optocoupler HCPL-3120 IC. It has two functions,

a) Amplification
b) Isolation

The Field Programmable Gate Array (FPGA) generates SPWM pulses for the control of inverter operation. The FPGA pulses are provided as inputs to the gate driver circuit. The gate-drive circuit is generally used to isolate and boost the input signal of the controller. The gate-drive circuit output is connected with the gate of IGBTs. The FPGA generates the SPWM it controls switches of proposed three-phase inverter at a switching frequency of 5KHz. Xilinx software is used to design SPWM code and then download it to FPGA through PC. ModelSim also used to verify that designed code is working properly. Modelsim simulations display real time operations of three phase SPWM. After assuring design code working properly then its download to FPGA board which control whole operation of proposed inverter and make sure pure AC output voltages.

Chapter 4

Software & Hardware Implementation

4.1 Introduction

This section outlines a systematic progression through MATLAB simulations, FPGA programming, Modalism simulations, and hardware deployment. Each step contributes to a comprehensive approach that bridges theory and practical application, culminating in the creation of a functional three-phase sinusoidal PWM inverter using FPGA technology. This section consists of four key steps that lead to the successful execution of the project.

The first step involves MATLAB simulations, where circuit diagram was developed and simulated using MATLAB tools. Following the MATLAB simulations, the project advances to FPGA programming. This programming transforms the theoretical concepts into executable digital logic, preparing the design for direct implementation on FPGA hardware.

The final phase of the project encompasses the hardware realization. At this portion, the FPGA-based design is physically implemented on the chosen FPGA hardware platform. Through this hands-on stage, the theoretical design is brought to life, enabling the observation of real-world performance and interaction with external systems.

4.2 Step of project

The project involves four steps

- Generation of SPWM using MATLAB
- Design Procedure on FPGA
- Modalism Simulations
- Project Hardware

4.2.1 Generation of Sinusoidal Pulse Width Modulation (SPWM)

SPWM technology is very popular in power converters. In sinusoidal PWM, the width of each pulse varies in proportion to the amplitude of the sine wave evaluated at the location of the same pulse. The carrier voltage Vc is compared with the signal Vr at the desired frequency by the comparator [18] as shown in figure 7. The output is high

when the amplitude of the sine wave is high, otherwise the output is low. Output comparison is done in a comparator pulse generator such that the pulse width of the output voltage wave coincides with the comparator pulse width [18].

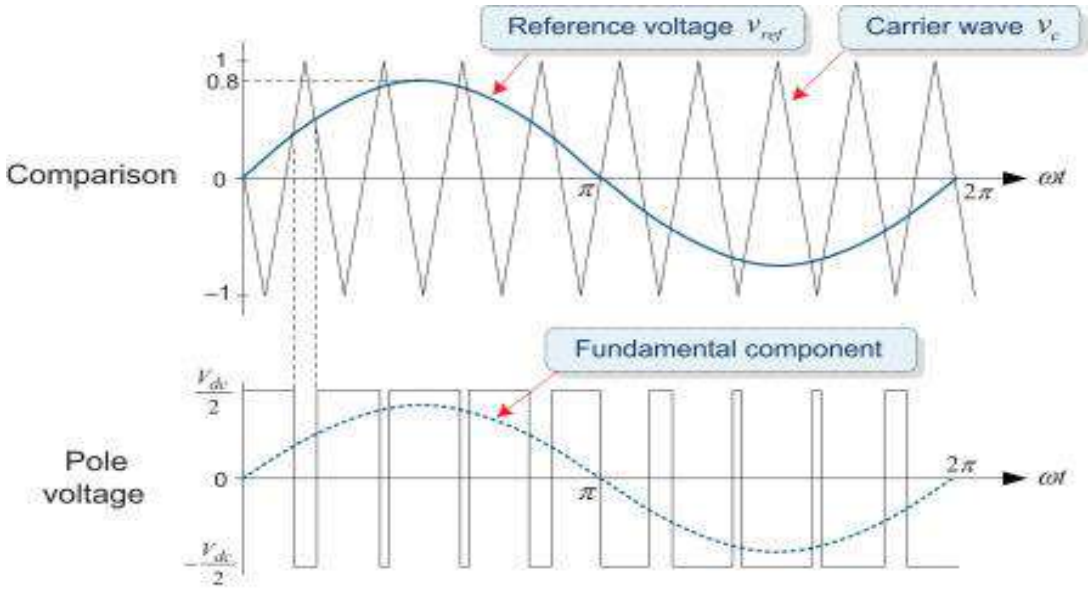

Figure 7: Sinusoidal PWM

SPWM Generator shown in figure 8.

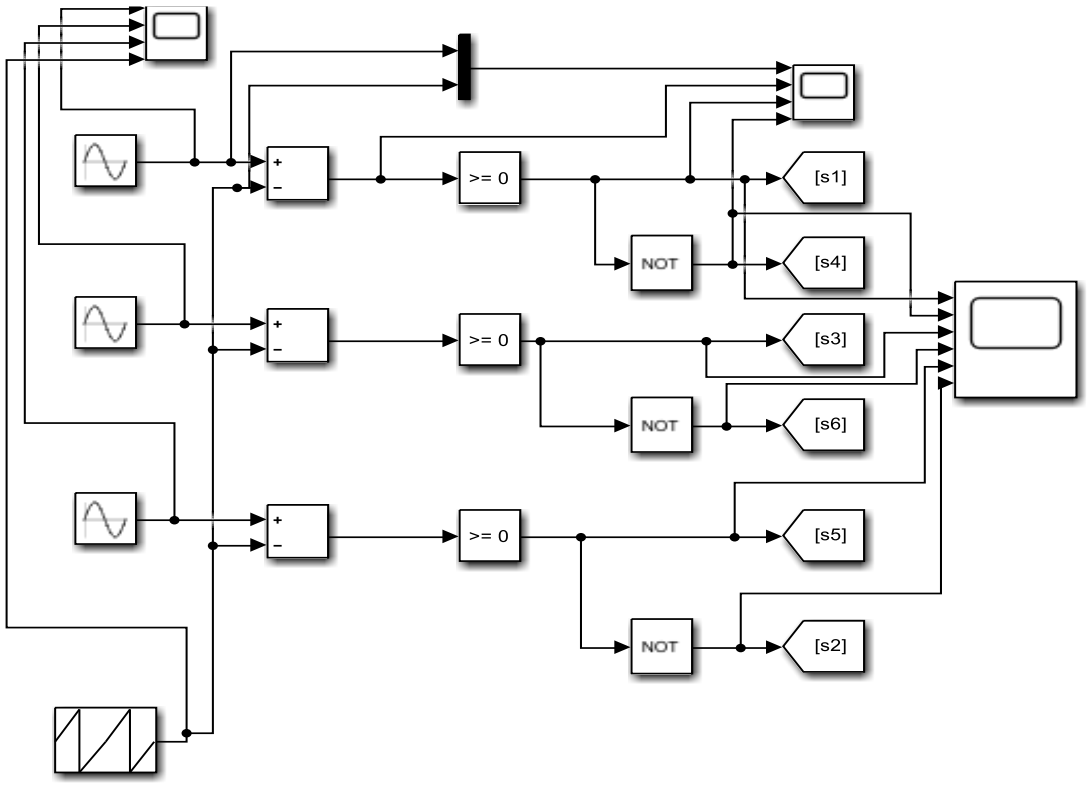

Figure 8: MATLAB SPWM generator

A triangular carrier wave is compared with the reference signal shown in Fig 3. Comparing the carrier signal with three reference phases produces gating signals respectively these are applied to upper switches (S1, S3, and S5) respectively and lower switches (S4, S6, and S2) [18].

The generation of SPWM is shown in figure 9. There are three sinusoidal reference waves each shifted by (120°).

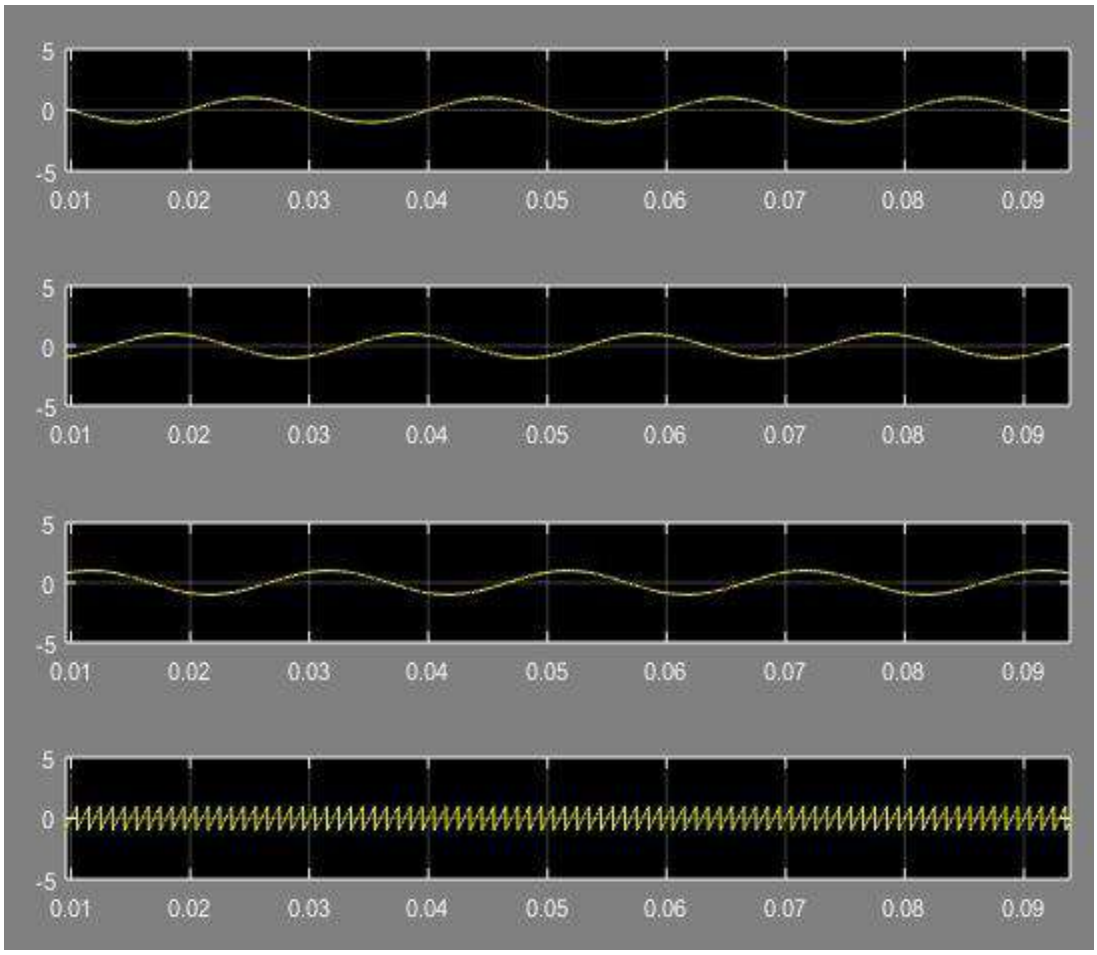

Figure 9: Input for SPWM Generation

Here, a triangle is compared to us using sine waves shifted by 120 degrees. SPWM generator output is shown in Figure 10. It provides a gate signal for the inverter to change according to the given frequency. The SPWM signal, which converts power to power in the inverter, is generated by comparing the three-phase sine wave with the same square wave.

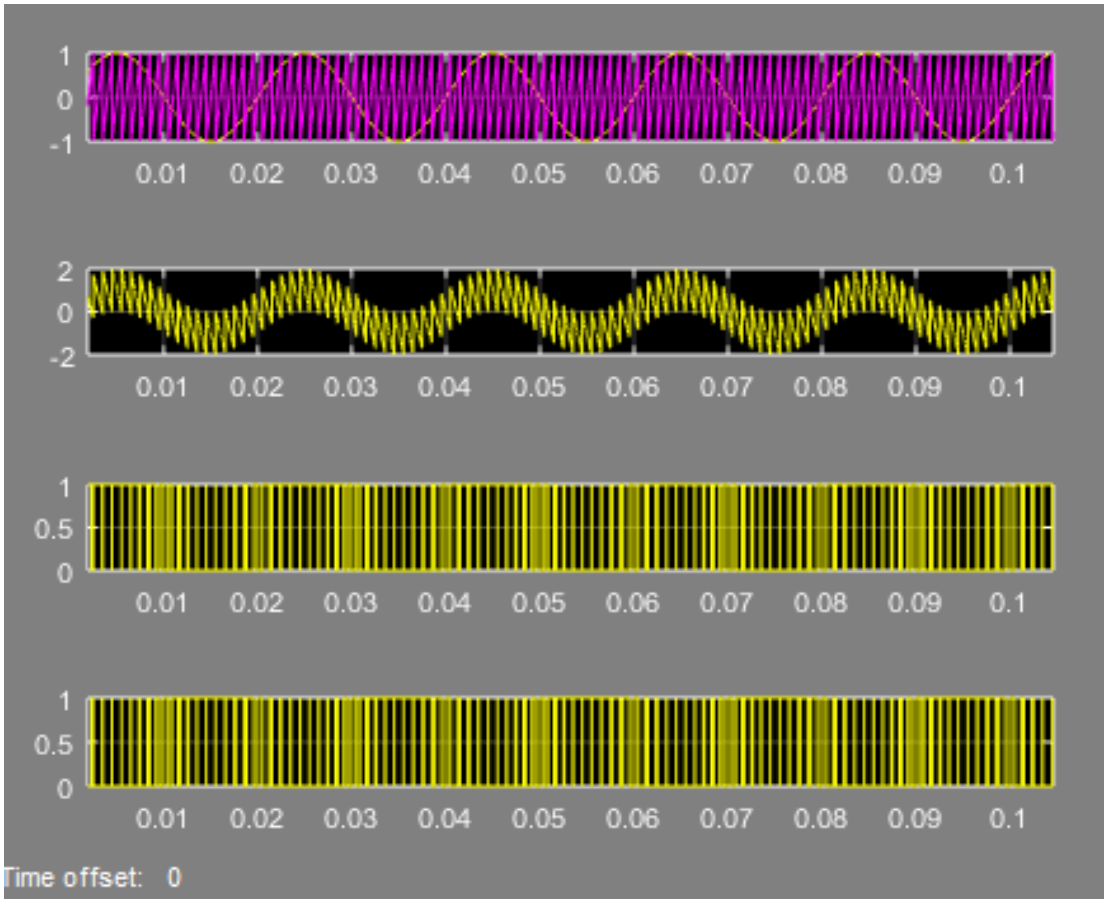

Figure 10: SPWM Generator Output Signal

4.3 Design Procedure on FPGA

Field Programmable Gate Arrays (FPGAs) are logic cells and junction arrays that can be reprogrammed as shown in figure 11. It can be build and change it when need to do. Its rapid production and low cost prototyping makes it suitable for embedded and advanced system designs. A field programmable gate array (FPGA) is used to generate the SPWM signal required for switching operation of the proposed inverter.

FPGA is becoming more popular as a result of its flexibility and ability to be designed again and again. In contrast to microprocessors, FPGAs are highly configurable and perform well.

Due to the extraordinarily broad range of applications that modern FPGAs can handle, they can be referred to as fully programmable systems on chips. When performance is taken into account, FPGA outperforms traditional processors in the following performance vectors: bandwidth for compute, memory, and input/output.

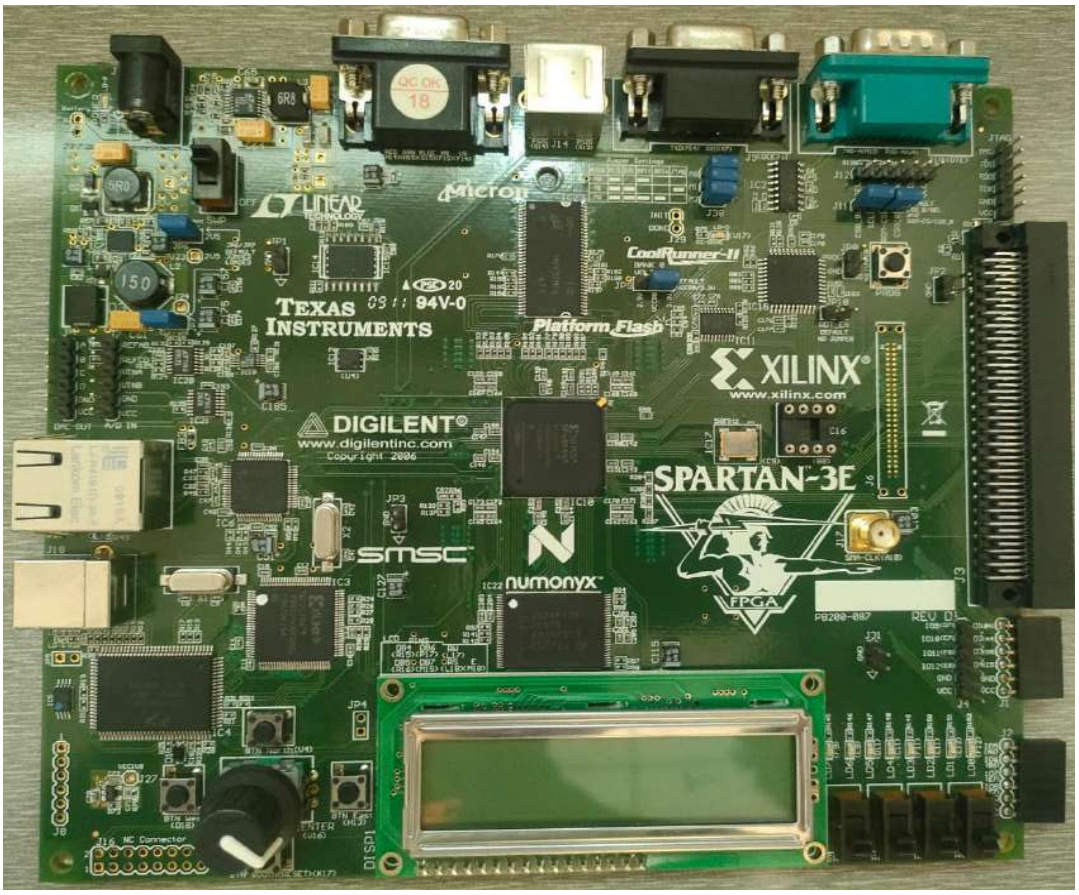

Figure 11: Spartan-3E Board.

4.3.1 FPGA Design Flow

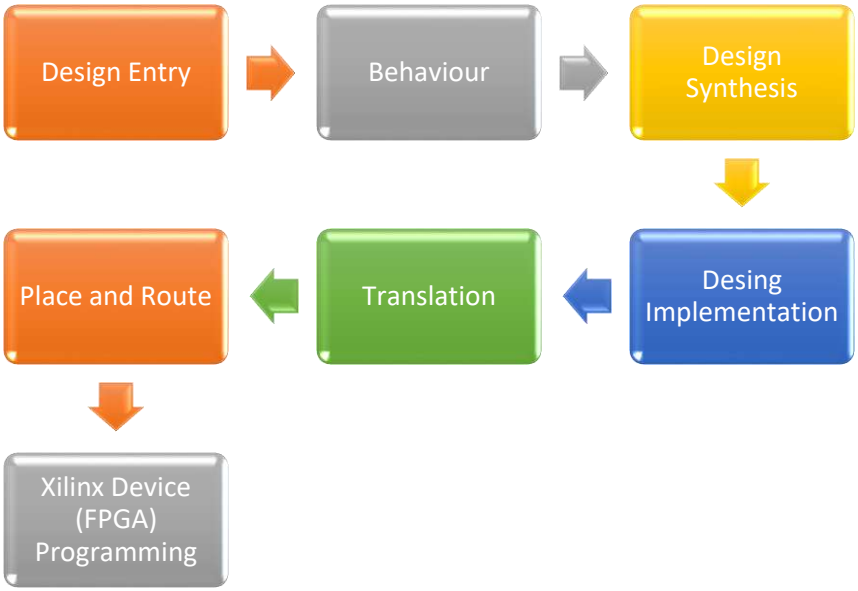

Figure 12: FPGA Design Flow

4.4 FPGA programming software

The program was called Xilinx ISE Project Navigator. Older software versions might be used; this guide utilizes version 14.2. The Xilinx website at http://www.xilinx.com/ under the Free License section has a download link for the program. Users must register and login. Figure 12 shows the flow of the project navigator, listing some of the usual functions and sub-windows.

A new VHDL project window is opened in Xilinx, Do syntax checks on the code, after you write it to ensure that the proper syntax was used in figure 13.

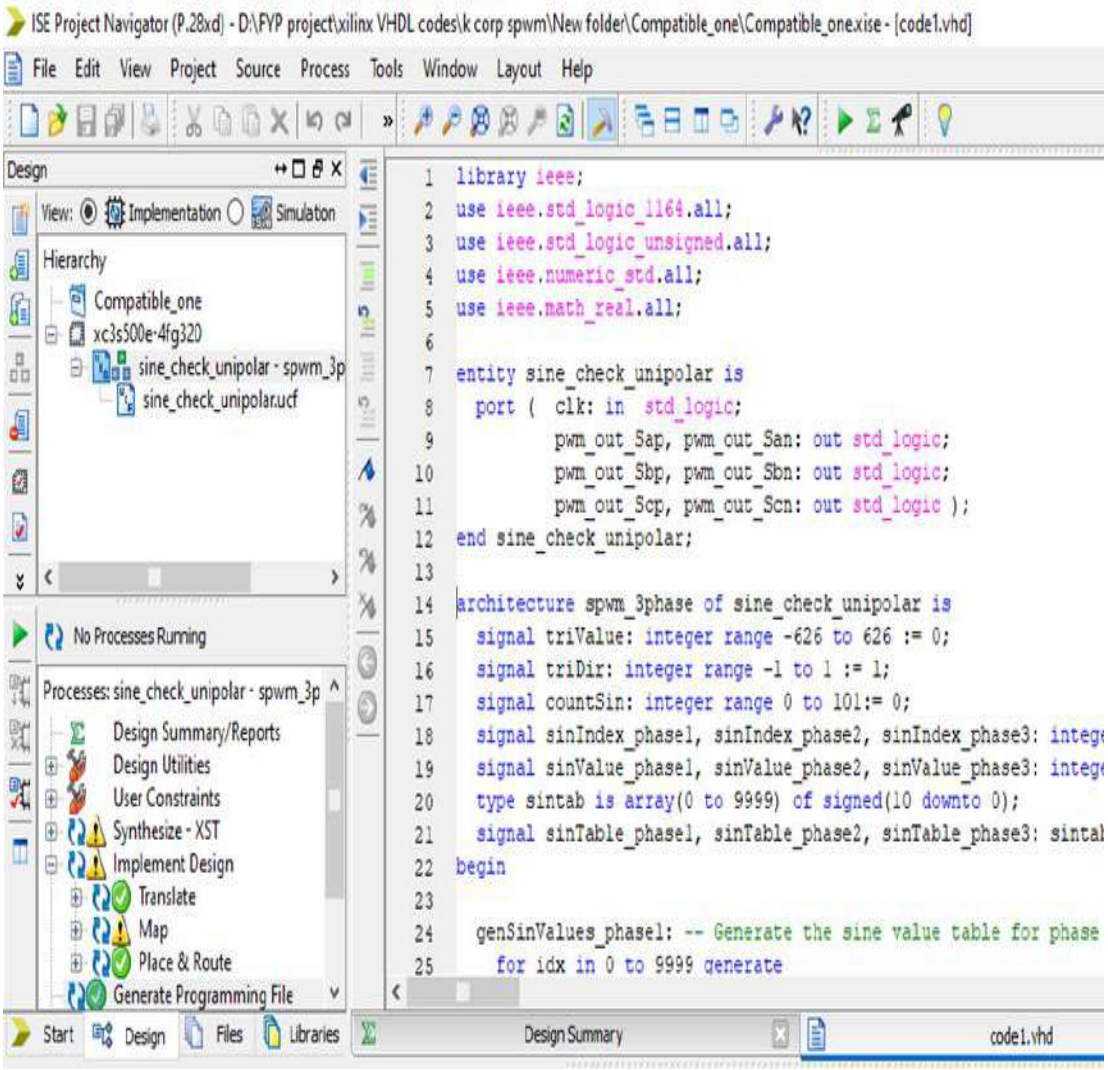

Figure 13: View of the Project Navigator software while running

4.4.1 Startup the Project Navigator software

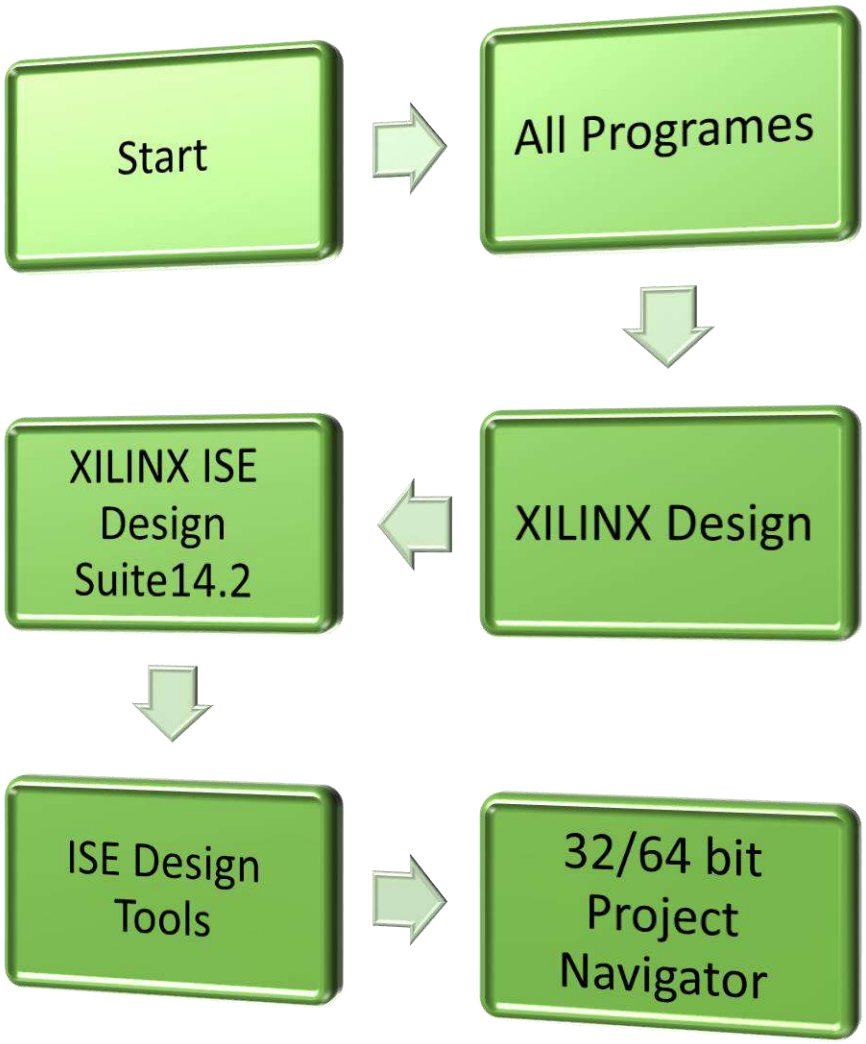

Figure 14: XILINX software block diagram

When the Xilinx Project Navigator software start.

The initially displayed window that opens up should look similar Fig 14.

1. Create a New Project
2. Select New Project File. The New Project will appear.
3. Type tutorial_1 in the Name: field.
4. Choose Location: and Working Directory: for your project.
5. Verify that selected as HDL.
6. The set as shown in Fig15.
7. Click Next for Project Settings page.

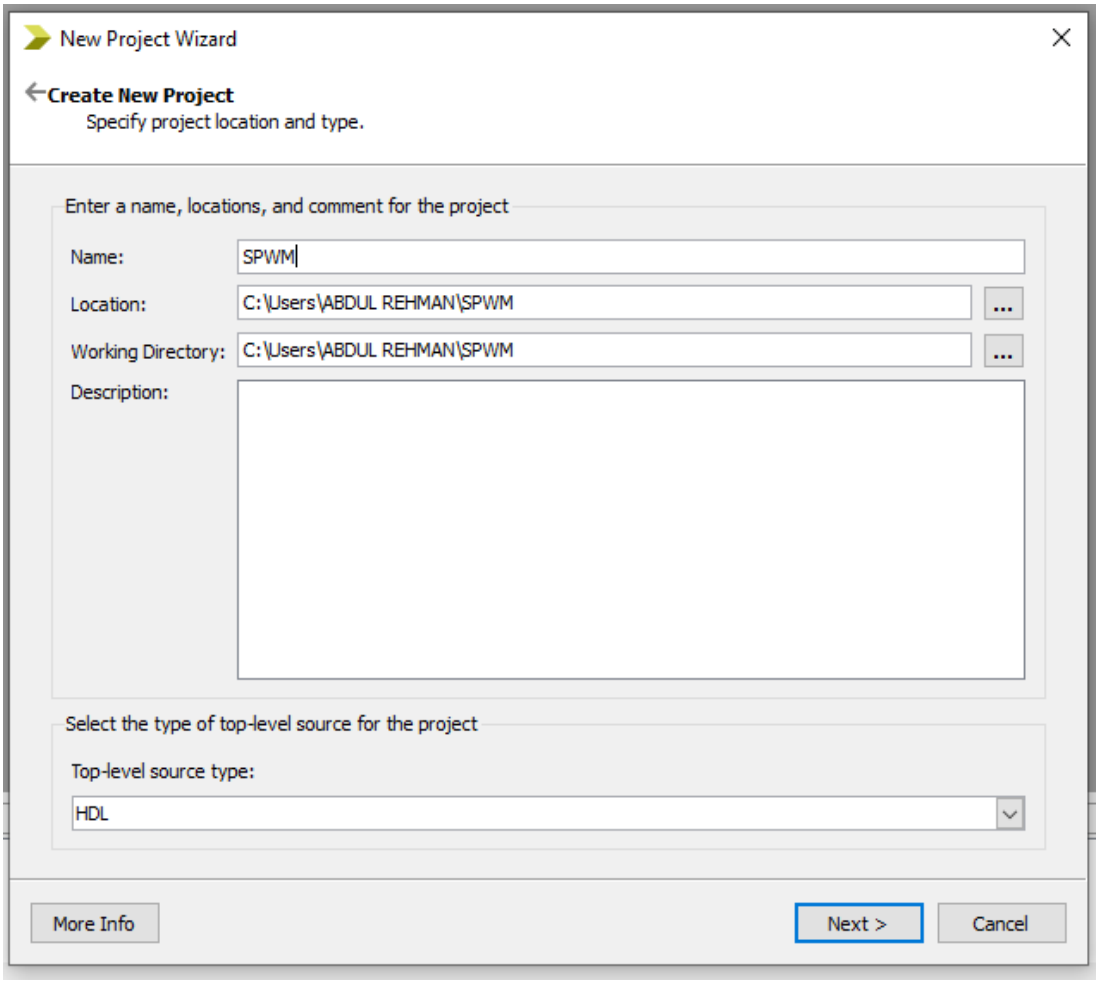

Figure 15: New Project Wizard, Create New Project Page

Assign the following properties:

- Category: All
- Family: Spartan3E • Device: XC3S500E
- Package: FG320
- Speed Grade: -4
- Source Type: HDL
- Synthesis Tool: XST (VHDL)
- Simulator: ISim (VHDL)
- Language: VHDL
- Specification in Project File: Store All Values
- Compile Order: unchecked
- VHDL Source Analysis : VHDL-93
- Message Filtering: unchecked

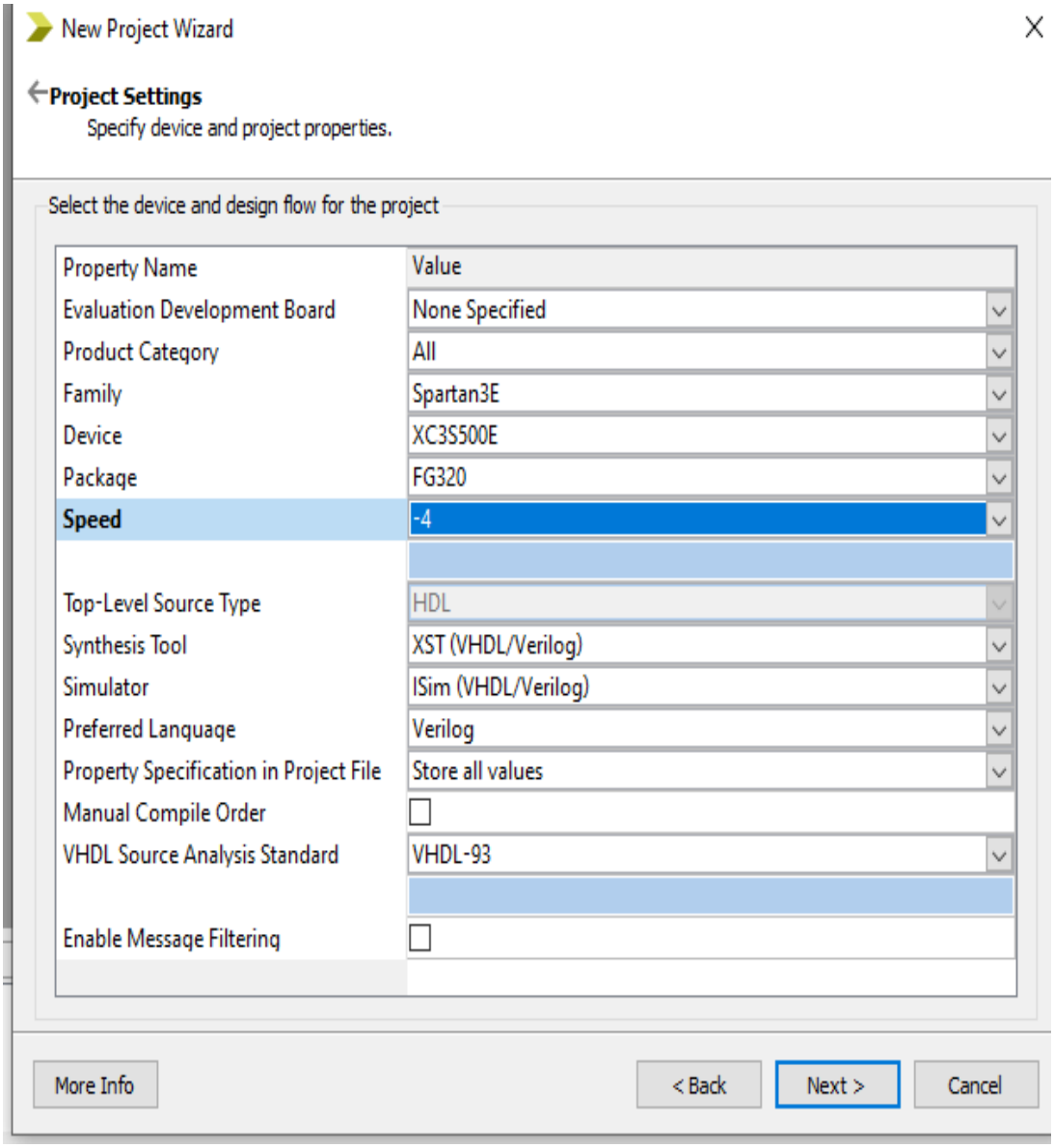

Figure 16: New Project Wizard, Project Settings Page

Properties filled in new project wizard, project setting page can be vary as per FPGA model.

Top level source can be HDL or VHDL as per requirements of designed system programming figure 16.

Other parameters will remain same even Verilog or HDL language is selected.

To proceed to the Project Summary screen, which will come up as seen in Figure 17, click Next.

Verify all properties in shown in project summary se per you selected in previous step.

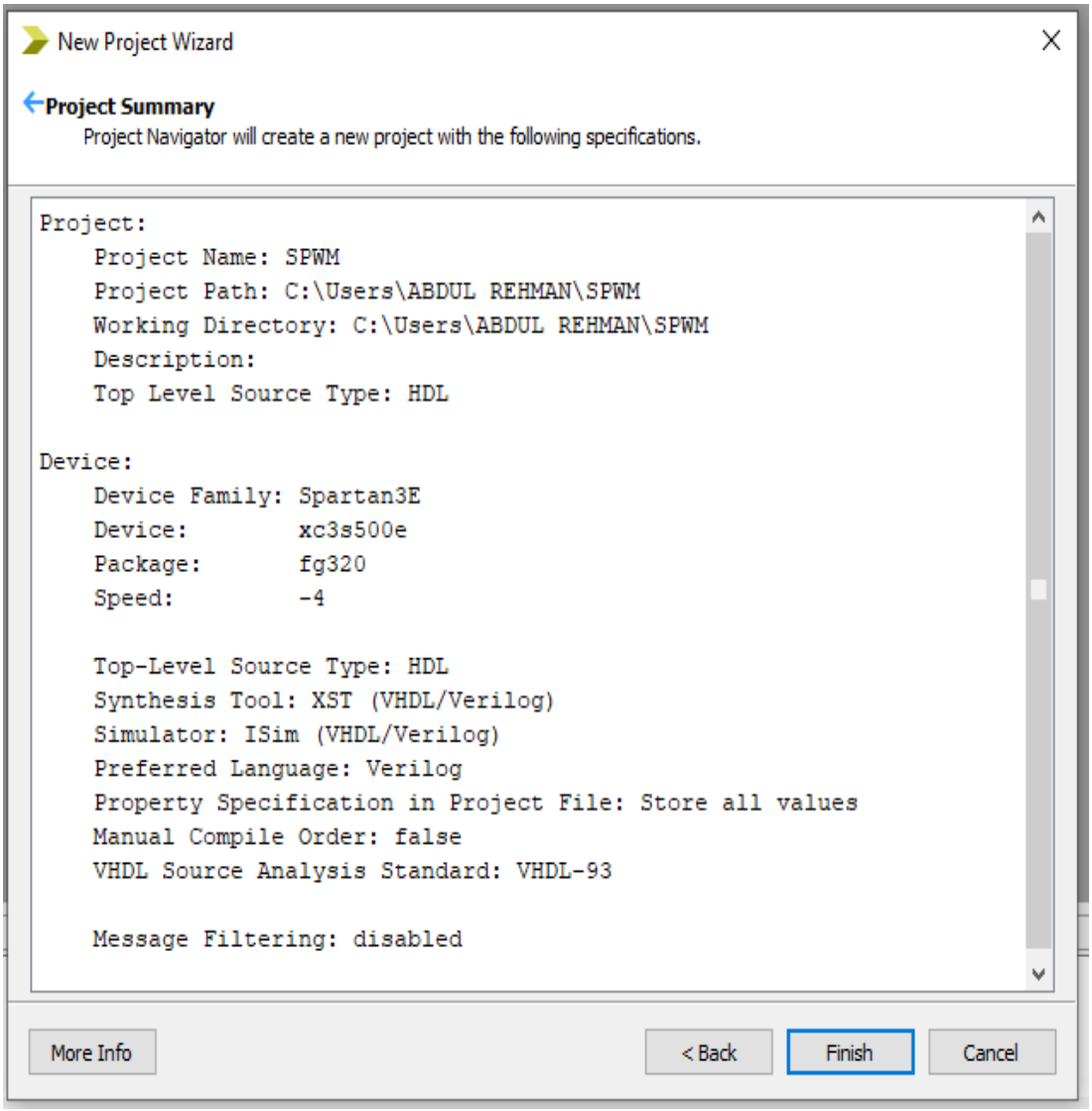

Figure 17: New Project Wizard, Project Summary Page

To close the New Project Wizard, click Finish. As seen in Fig. 17.

4.4.2 Adding a New VHDL Source

1. Choose New Source as seen in Fig. 18.
2. The source must be set to VHDL Module.
3. Enter the file name and location, keeping the project location and file location the same.
4. Make sure the Add to project box is checked.
5. As seen in Fig. 19, the New Source Wizard now appears.
6. Click on New Source follow above steps.

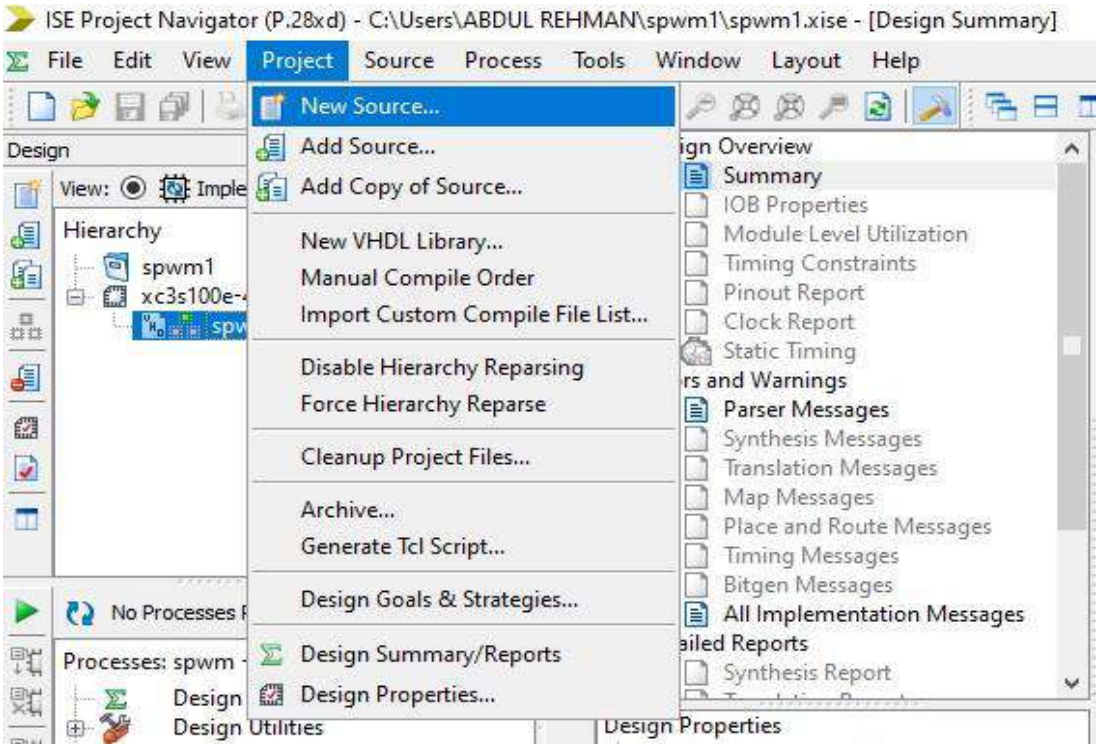

Figure 18: Adding a new source file to the project

Now, the New Source Wizard open as seen in Figure 19.

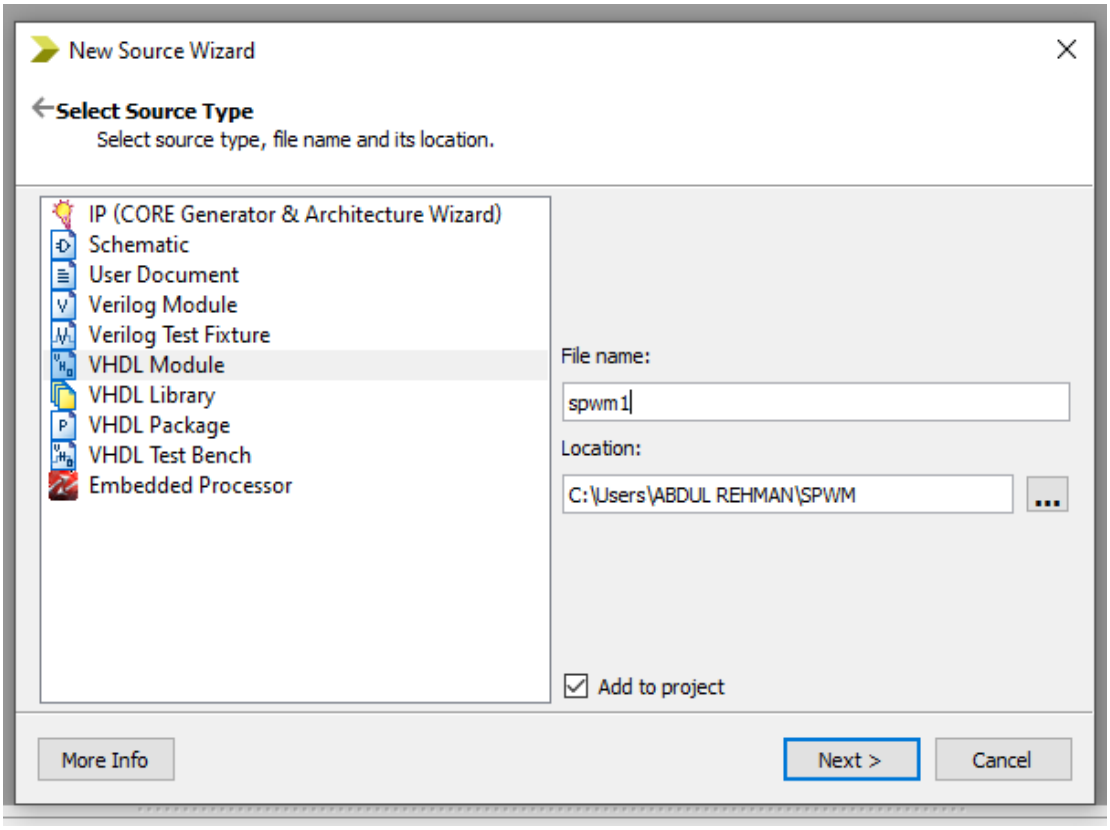

Figure 19: New Source Wizard, Select Source Type

7. Click Next to go to the Define Module window.

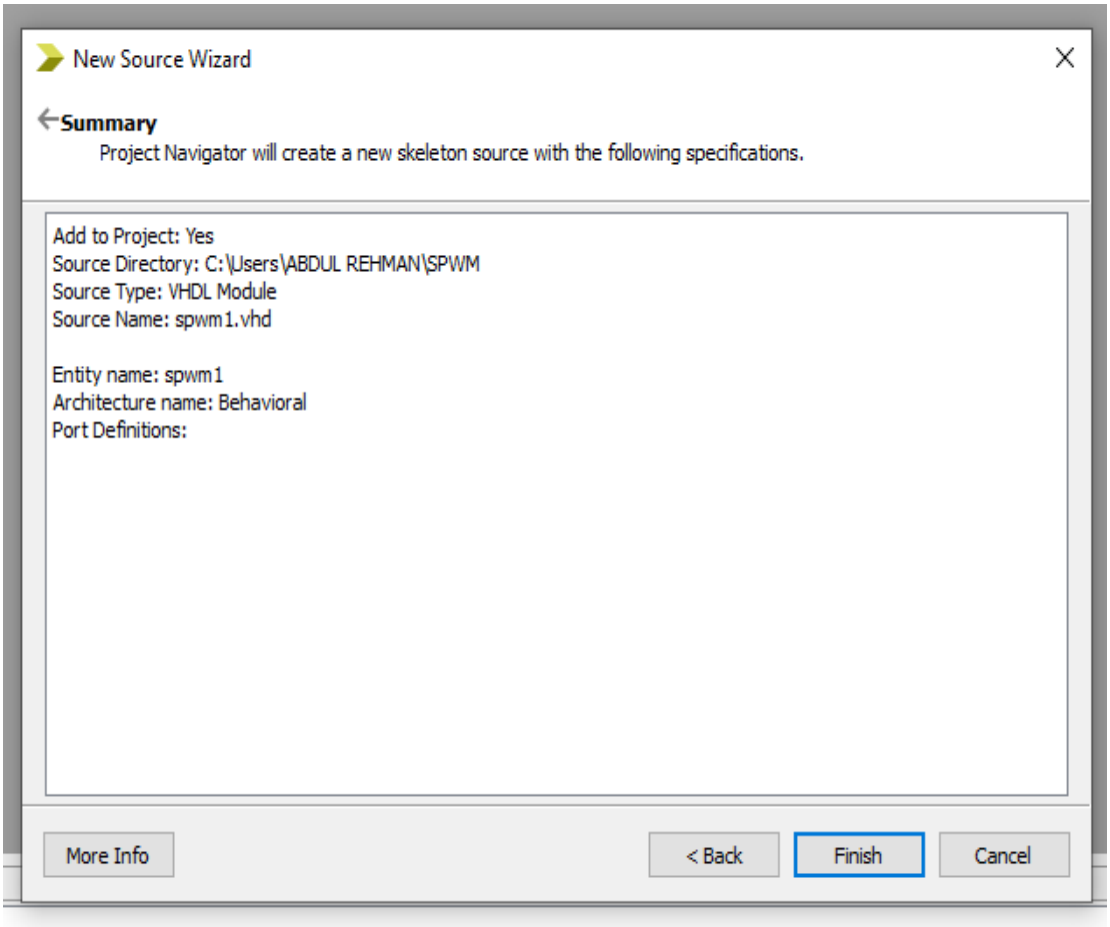

Figure 20: New Source Wizard, Summary

Figure 20 shows that Press Finish. Thereafter, SPWM will show up in the Sources box. When SPWM is double-clicked in the Sources window, SPWM.VHDL is shown in a tab.

4.4.3 Synthesize, Translate, Map, and Place & Route

Synthesis, translation, mapping, insertion and routing follow steps. These steps are included in the Xilinx software and are briefly described below:

• Synthesis: Create a list for each file.

• Translation: Put too much information in one list.

• Map: The map created for slices and I/O blocks.

• Placement and approach: Decide where your design will be placed on chips and components. Before changing the

Design, write a User Restriction File (UCF) to assign the FPGA pin configuration to the SPWM generator I/O. When done, Interpreter will merge this UCF file and the netlist created after linking to the Xilinx design file. Mapping is to match the design with the available resources of the target FPGA device.

The place and path used to incorporate the logic of inserting the design's building blocks into the FPGA and putting them together so they take up the least amount of space and satisfy the deadline are the last steps in the design process.

This function creates NCD output files. Figure 21, click the "+" sign next to construction if it is not yet expanded. This will present the "Change", "Map" and "Location and Route" stages.

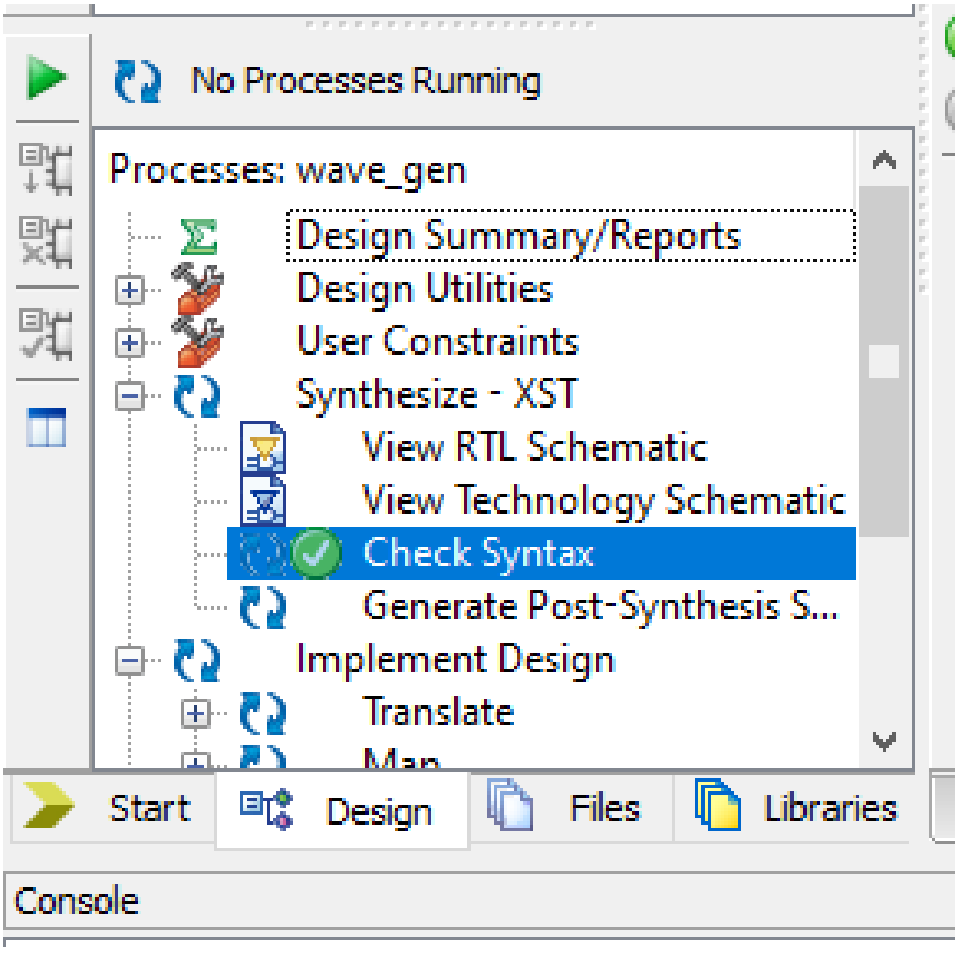

Figure 21: Portion of Project Navigator screen, with Implement Design expanded

Now double click to apply the design. This will cause Synthesize - XST to run first. Then Translation, Maps and Places and Routes will run sequentially. A green checkmark will appear next to each level when completed. After these steps are completed, the project navigation screen will appear as in Figure 22.

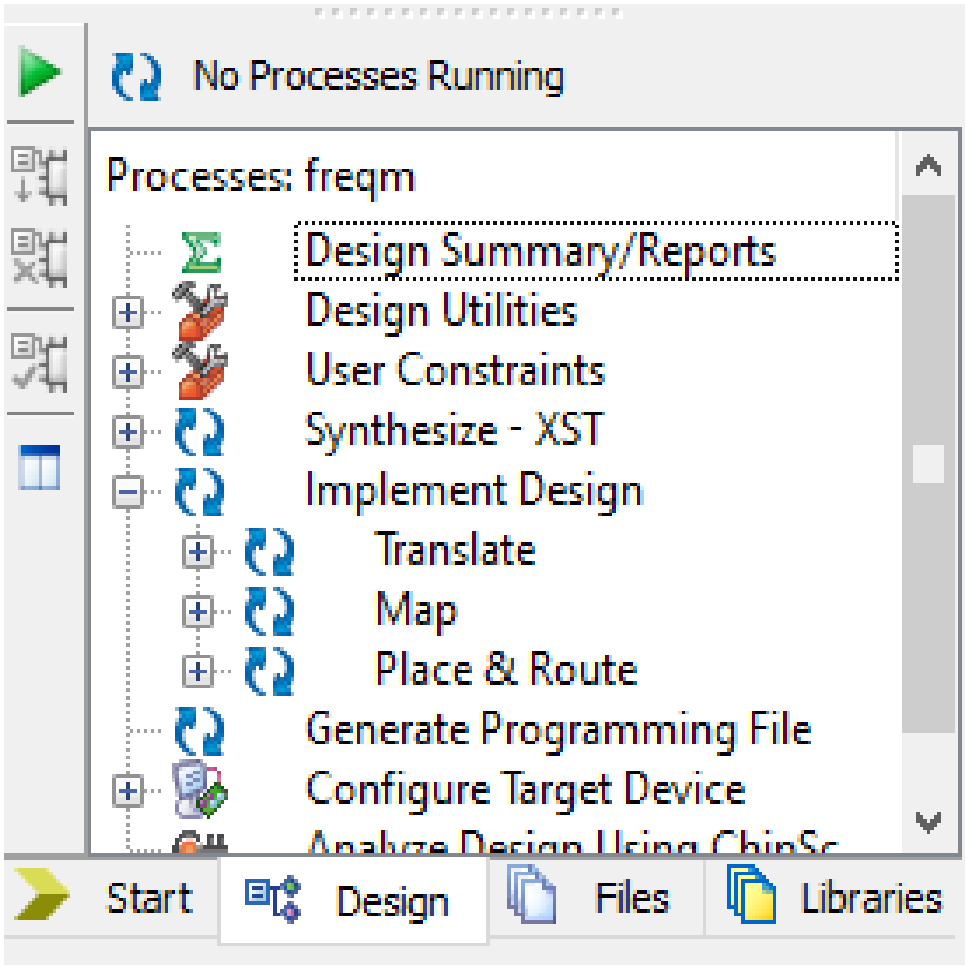

Figure 22: Portion of Project Navigator screen, with Implement Design expanded, after Translate, Map and Place & Route

4.5 Download Design to Board

The programming file is created from the process tab of Xilinx ISE, which converts the encoded data to BIT file after routing it. The Xilinx device generates the bitstream for the FPGA configuration. This BIT file is used download to the FPGA.

1. Click the "+" sign next to the target setting as shown in Figure 23. This will expand to reveal the Impact Product Management (IMPACT) option.

2. Click Create Programming Files.

3. Make sure the green icon appears after the process is complete.

4. Attach the data wire and power adapter to the FPGA card. Make sure the Sparan-3E card is activated and connect the data wire from the FPGA card to the PC.

The run faild map as shown in fig.19 the Portion of Project Navigator screen, for Generate Programming File.

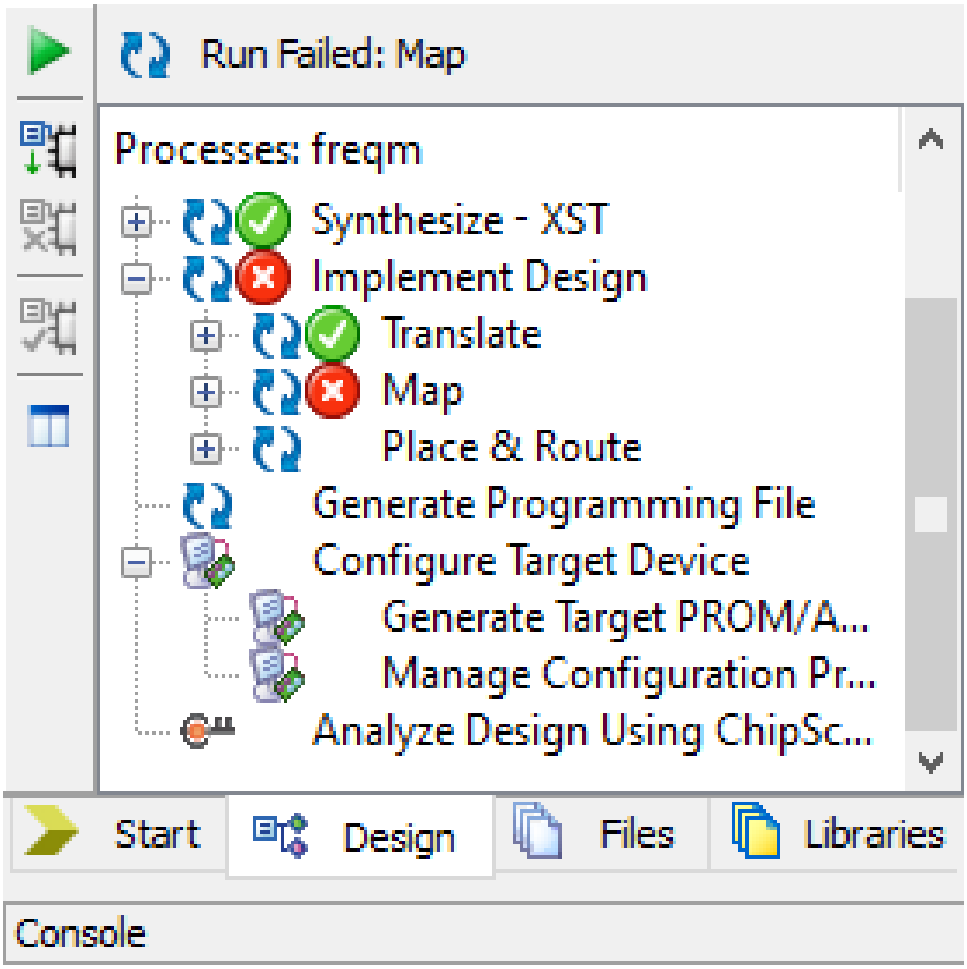

Figure 23: Portion of Project Navigator screen, for Generate Programming File

4.6 Configuring Target Device

Xilinx ISE has a "Create Target PROM/ACE" option under the "Process" tab to convert BIT files to PROM or ACE files. PROM or ACE data can be loaded directly into FPGA memory. By changing the UCF file we can assign different values and see how the FPGA output changes. This entry can be obtained by changing the code number assigned to the SPWM generator entry in the UCF file. The output can be seen from the LED assigned to the pin number of the SPWM generator output.

4.7 Modalism Simulation

Mentor Graphics created a tool called Modeling Fundamentals to mimic VHDL and Verilog designs. It is the simulation that is utilized the most in both business and education. Simulation is an important step in designing FPGAs. The simulations allow the designer to stimulate their designs and see how they respond to simulation.

4.7.1 Using Modalism for Simulation

Open Modelsim Starting window looks like Figure 24.

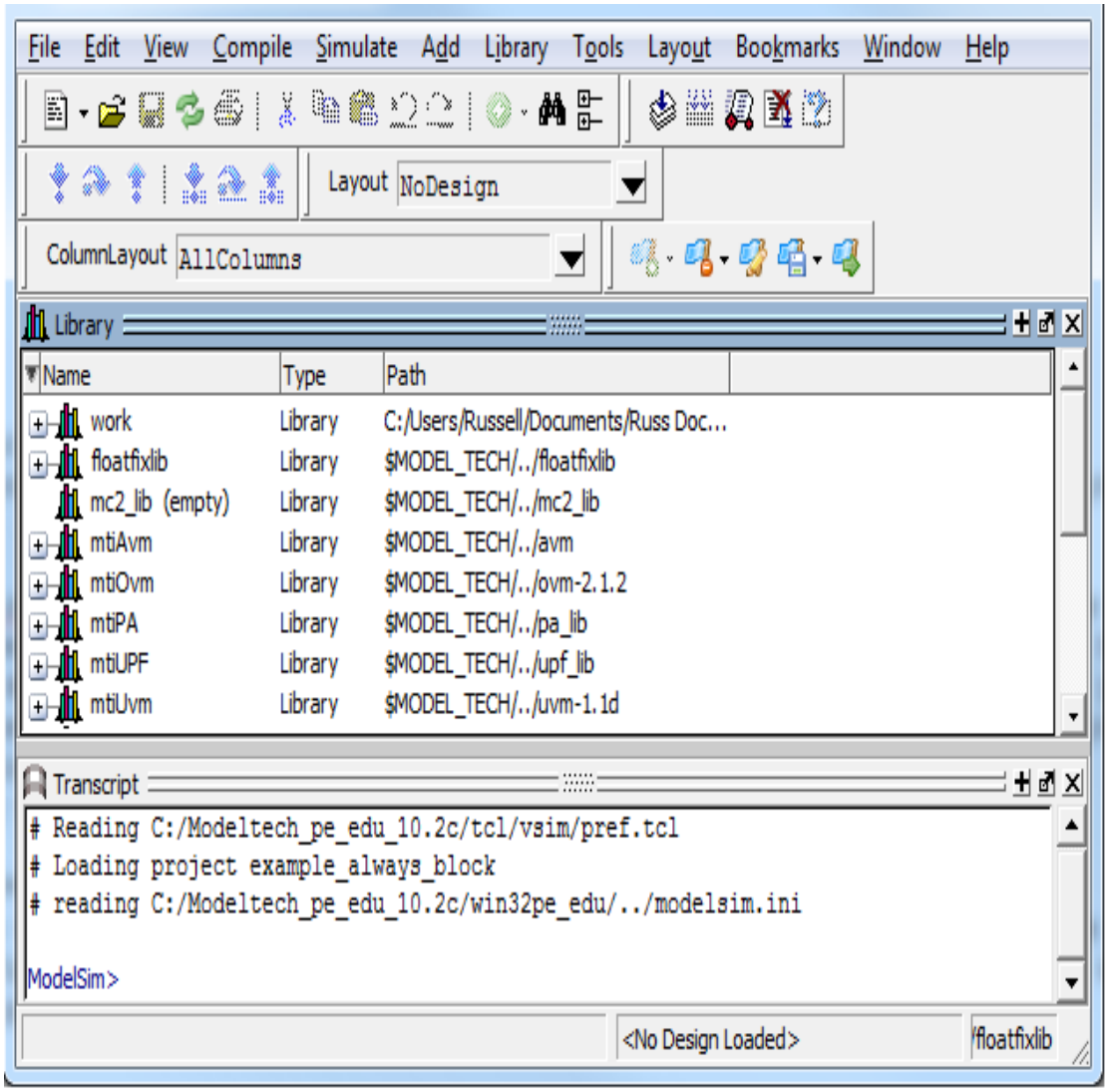

Figure 24: Modelsim Main Window

Now need to create a project in order to execute simulation.

Figure 25: Flow diagram to run the file in ModelSim software

The window shown in Figure 26. New project should have a location, a name, and a port. The .prj file extension is used by projects in ModelSim. Leave all other settings alone.

All code will be compiled into a "working" library, which is all that this phrase really implies [19].

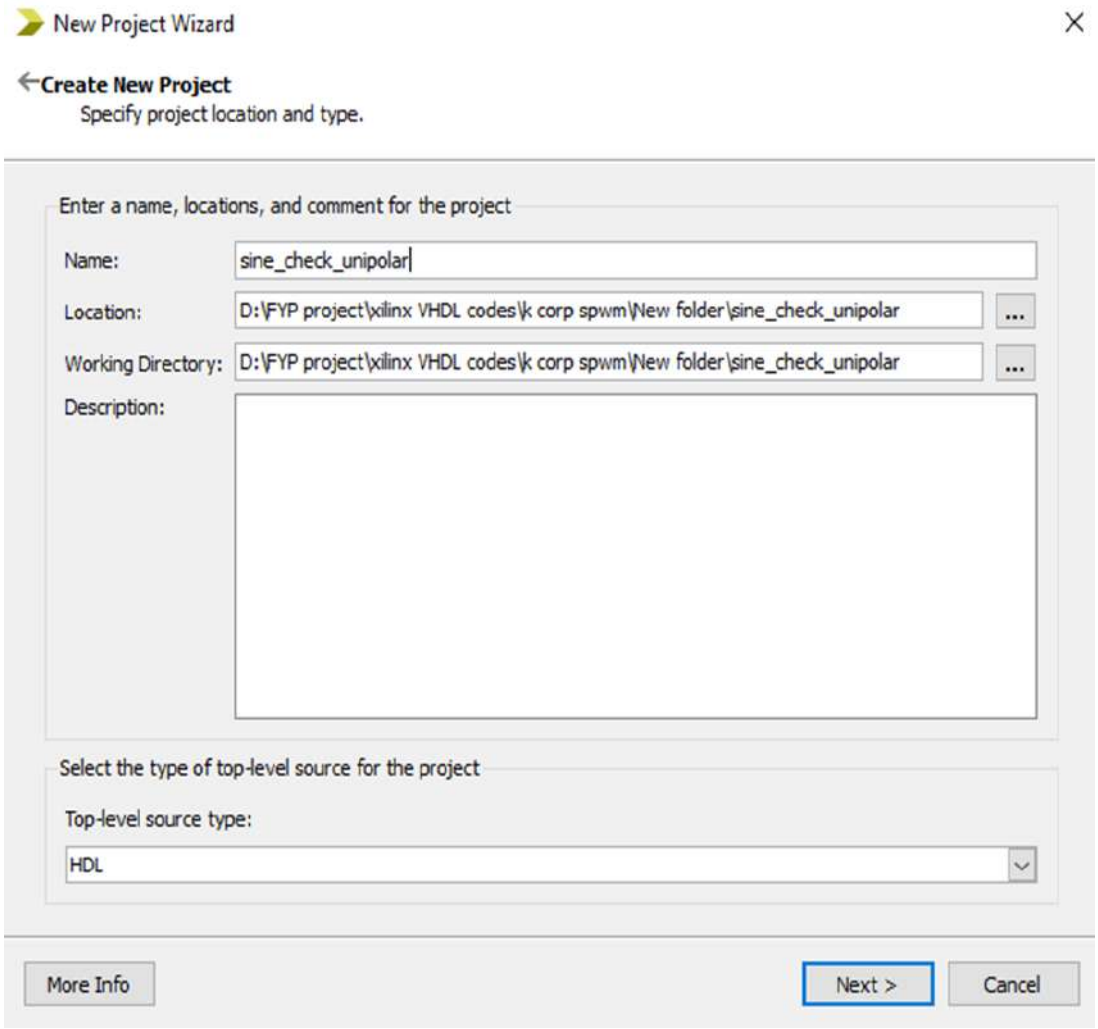

Figure 26: Create Project

Click Add Key Files as shown on the right side of Figure 27.

Go to the location of the gate.vhd vegate_tb.vhd you downloaded and add these two files to project.

Leave all other options unchanged. When done, click OK.

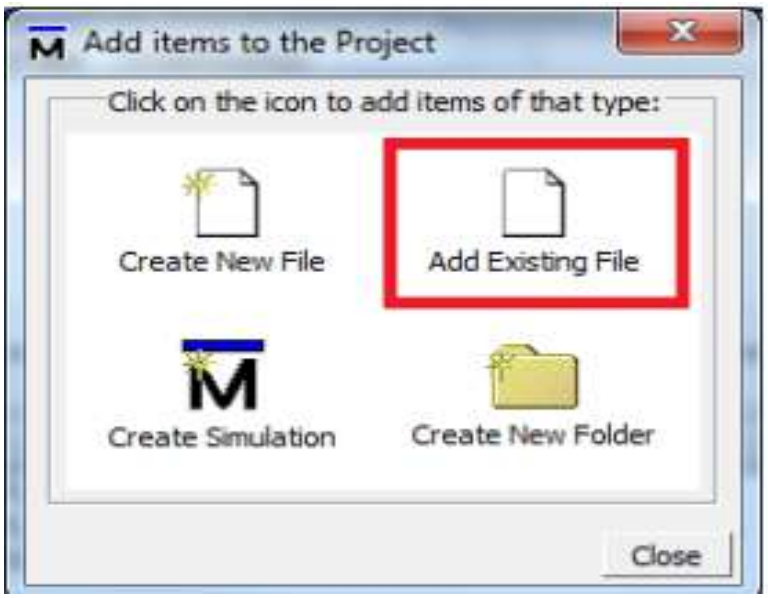

Figure 27: Add File

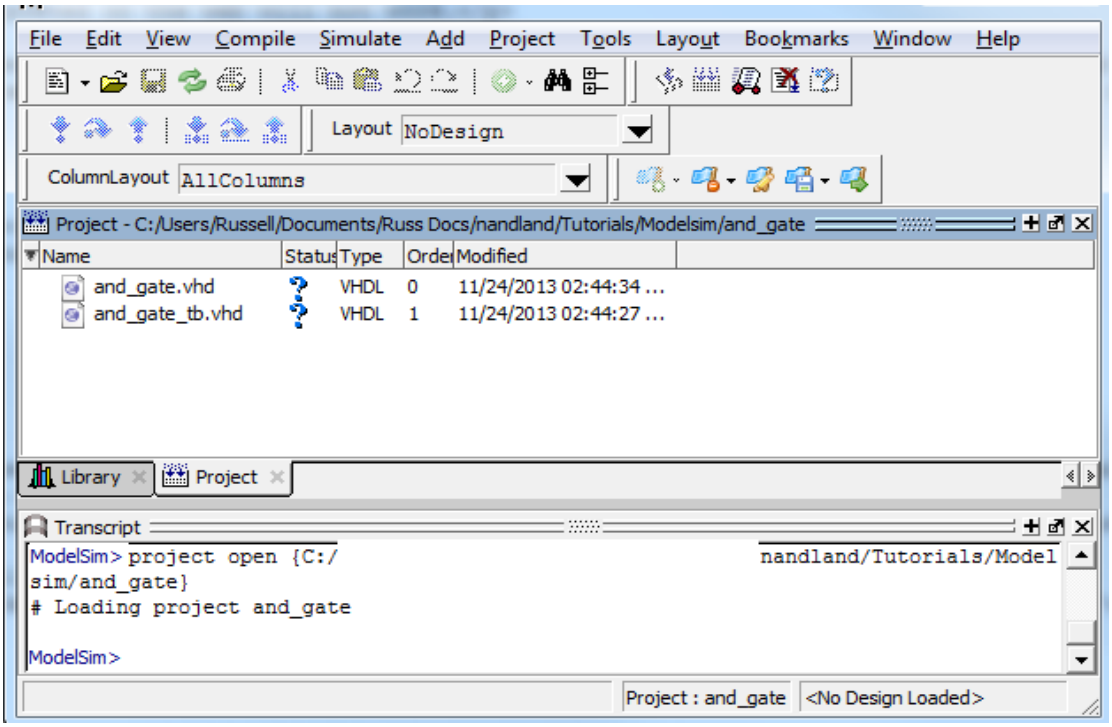

Figure 28: ModelSim Project Window – Files Added to Project

Now confirm that all of the data for project is accurate. View Figure 28 in the ModelSim project window above and pay attention to the two blue dots. This indicates that ModelSim does not gather this data. Must provide the location details. Click Compile from the context menu of the right-clicked and_gate.vhd, followed by Compile All. Should see a green message in the console window that the build is complete, as shown in the screenshot below Figure 25.

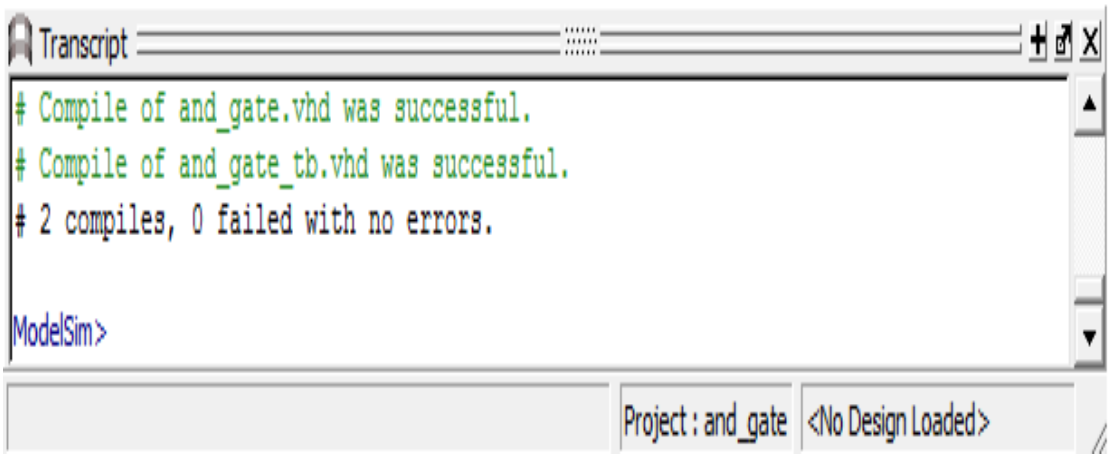

Figure 29: Result of a Successful Compile

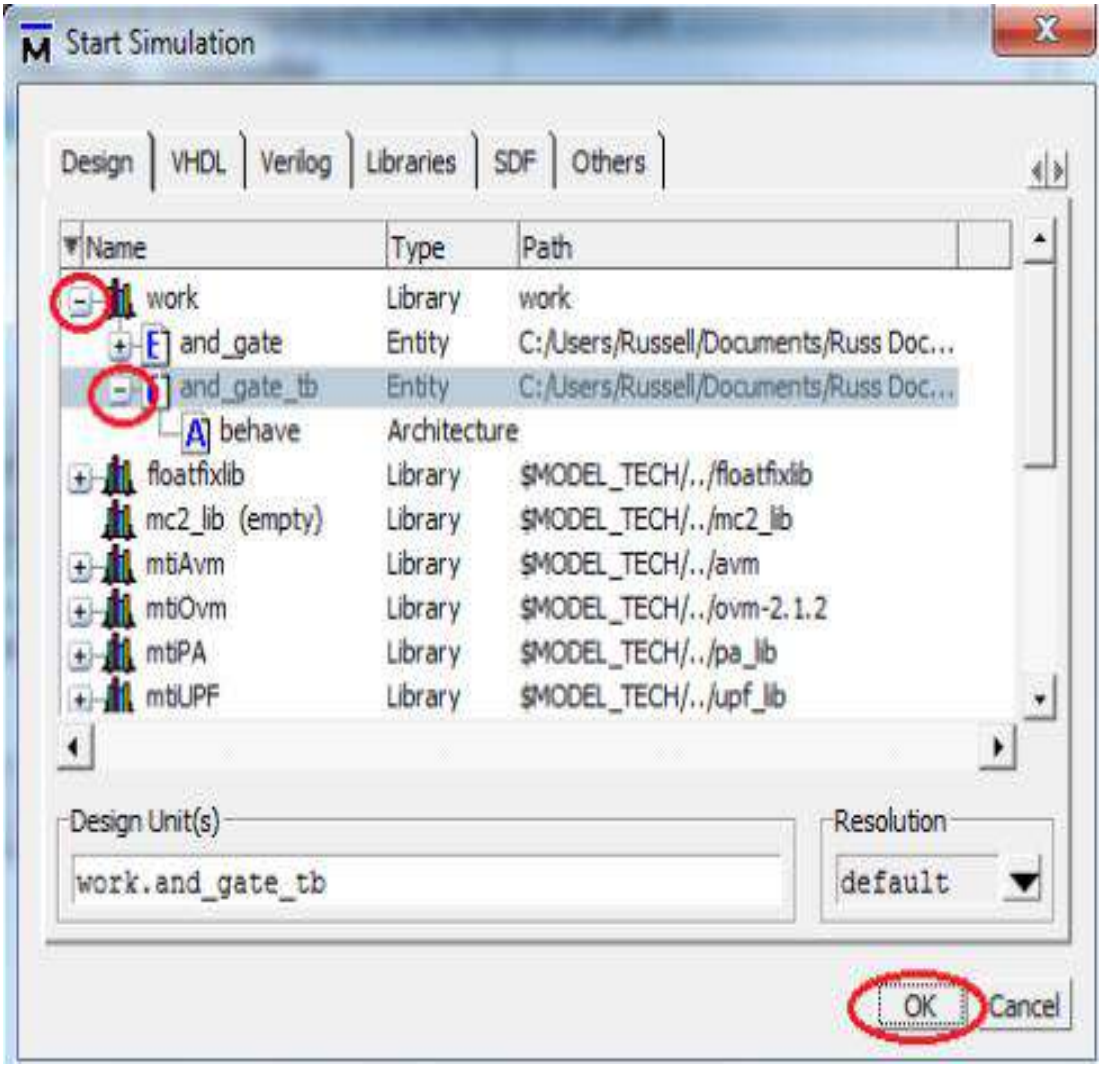

Figure 30: Start Simulation

To begin the simulation, select "Simulate" from the menu bar as seen in Figure 30. Then choose Simulation Start. The "Start Simulation" window will then be shown. Select the task, then select and_gate_tb by selecting the + sign next to it. Remember that since we are resembling the testbench level's architecture, select and_gate_tb rather than and-gate. With and_gate_tb selected, click OK.

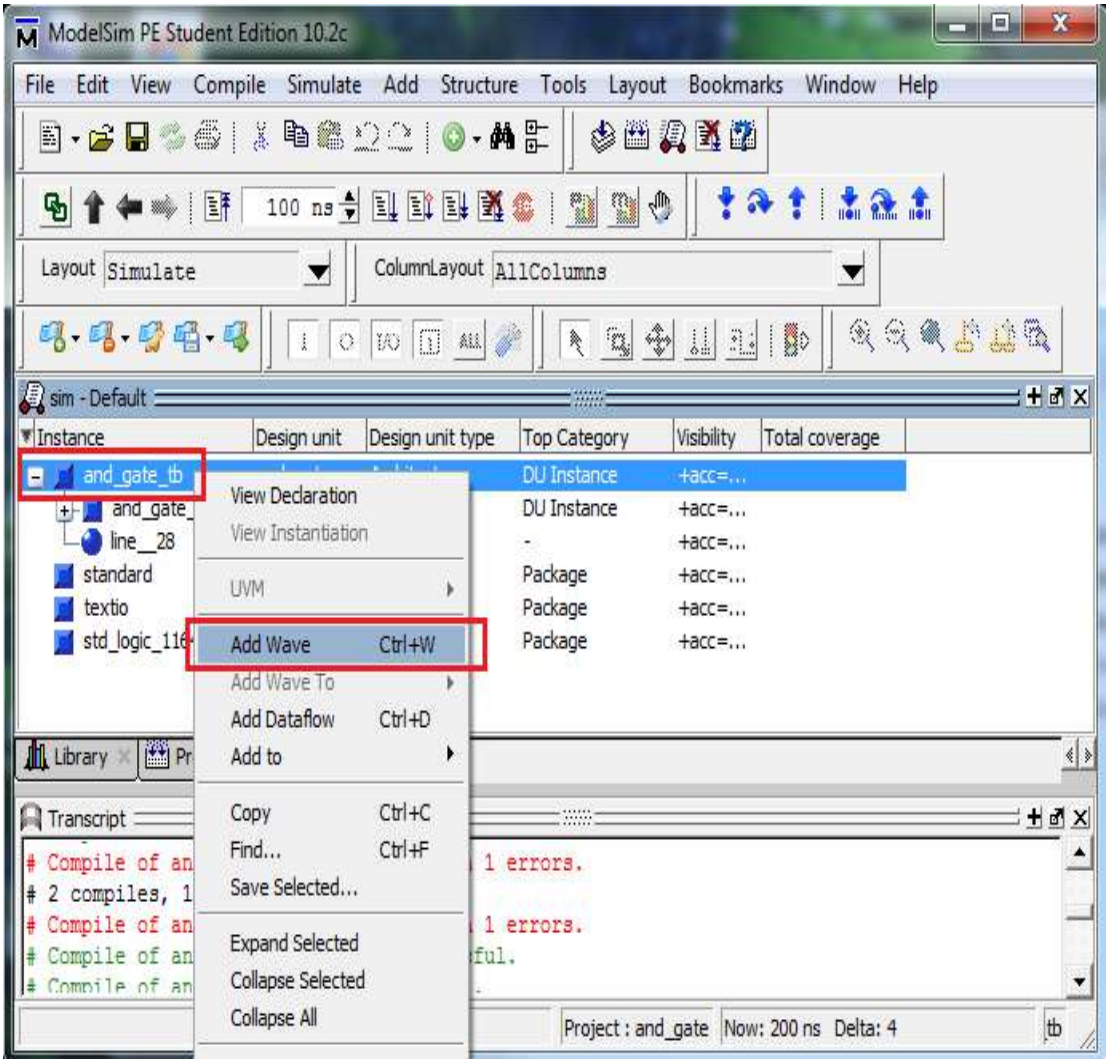

Figure 31: ModelSim Simulation Window – Simulation Ready

Figure 31 shows The model is prepared. The waveform view in ModelSim right now. The waveforms for each symbol in the format—binary 0s and 1s, hexadecimal numbers, binary numbers, enumerated kinds, etc.—are displayed in the Waveform View. It displays how your module reacts to various stimuli. The waveform is depicted in the graphic below, but before can see it, must add a few symbols to look out for. In this illustration, keep an eye on every signal on the test bench [19]. In the test window,

right-click and_gate_tb and choose Add Wave from the menu. Click and drag a signal from one window to the waveform window in modelsim.

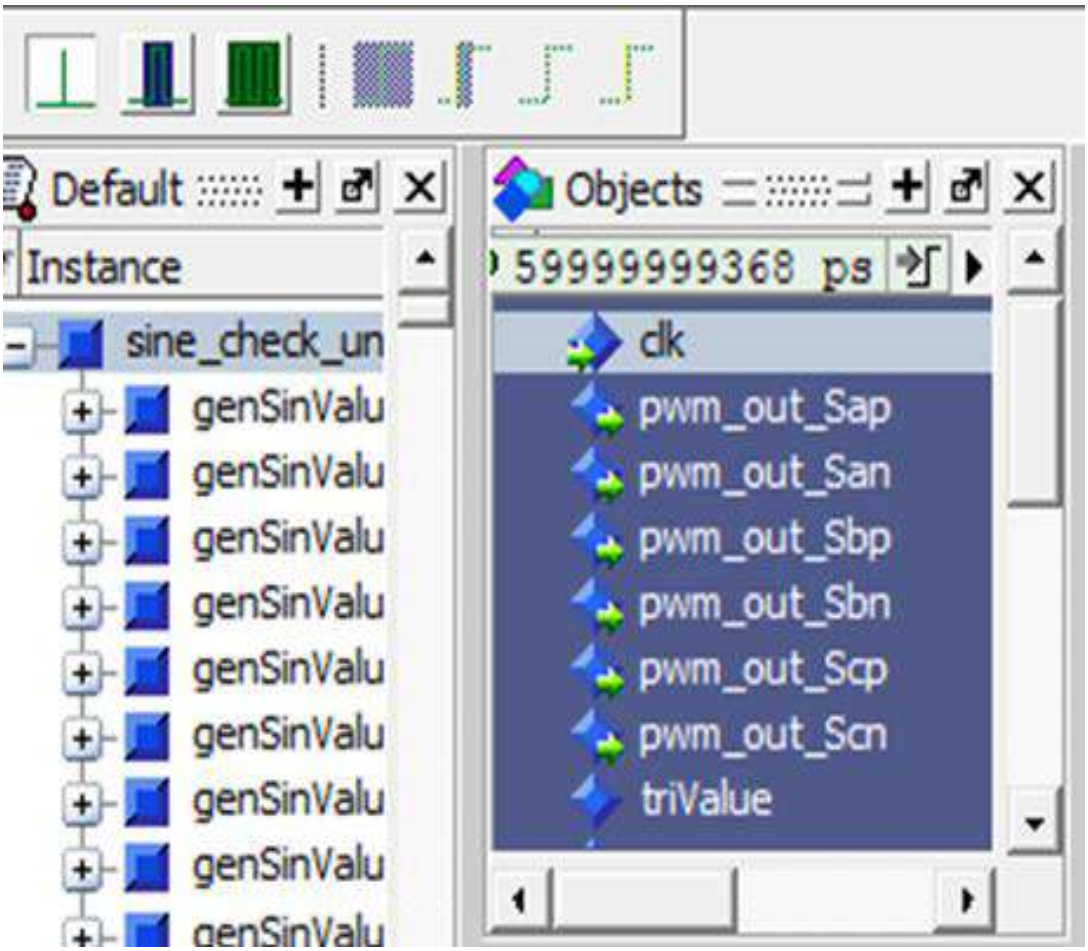

Figure 32: Wave Form

Here is waveform window in Figure 32. There are indications for each bench measurement. Click on the symbol with a little note and a downward pointing arrow next to the 200 ns time to start the simulation. Simulation will continue for 100 nanoseconds as a result. First ModelSim simulation has been produced.

4.8 Hardware Implementation

This part of the chapter presents the design details of a field programmable gate array based high gain coupled inductor diode assisted three phase boost inverter. In this inverter idea, the average DC voltage is raised with a pair of inductors and four diodes is connected in this way to prevent short through. To strengthen the DC-AC conversion and lower switch voltage, a tiny capacitor is added in parallel to the input terminals.

The main purpose of this study is to describe new inverter topology and control the algorithms developed in this paper.

The hardware consists of several steps.

- Inverter design.
- Power Circuit
- Gate Drive Circuit
- Isolated Power Supply
- Coupled Inductor Design

4.8.1 Inverter Design

Construction of a High Gain Coupled Inductor Diode Assisted Three Phase Boost Inverter is briefly described below.

Specifications:

1. Voltage rating 90Vdc input.
2. Current rating 5 A.
3. Switching frequency =5 KHz
4. All the devices in the inverter are isolated and have separate driving circuits

Sinusoidal PWM control signal for inverter switches comes from outside via FPGA board. The main functions of using an inverter are to produce stable AC power. FPGA generate SPWM signal which provided to the gate drive board also the isolated power supply is connected with the drive circuit. Gate drive boost the SPWM signal and provide it to switches of inverter. SPWM generation by FPGA, diode and inductor connection design is an important part of the project.

4.8.2 Power Circuit

To form a three-phase inverter, the power circuit consist on six IGBTs and three power diodes, two capacitors, a DC source, a gate drive board and a power supply to the board. Power circuit is shown in Fig 33. Power circuit provide isolated path for high input DC power and then converted power AC power filtered by power circuit. Power circuit is completely separate from control circuit therefore FPGA board remain safe from high voltages. Power circuit is main part of three phase inverter. One side of power circuit is connected with DC input and another side is connected with AC Load.

Figure 33: Power Circuit

- **Selection of IGBT**

Table 4: IGBTs have been the preferred device under these conditions

Low frequency circuit
Low frequency (<20 kHz)
Narrow or small lines or switching frequency
High voltage applications (600V)
Allowed to operate at high temperatures (> 100°) C)
5kW output power

The maximum output voltage is about 200V and considering the maximum input voltage of the device is selected as 600V. The allowable current that the device must conduct is approximately 5A.

Input DC positive and negative terminals connected with six IGBTS as shown Fig 34 Gate drive circuit output connected with the gates of IGBTs.

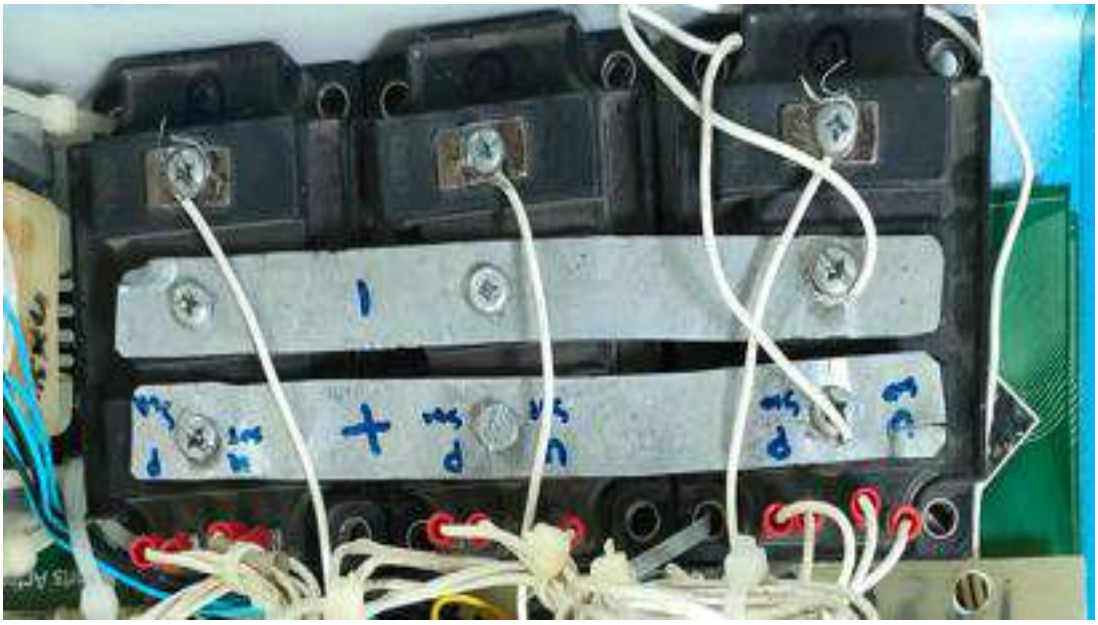

Figure 34: IGBTS Hardware Connection with DC input and Drive Circuit

4.8.3 Power Diodes

The main function of power diodes is to prevent short circuits in switches of the inverters. In this case of three-phase inverter, the diodes are connected to the DC link voltage, the maximum current can be up-to 20A for the diodes, and a diode with a rated upto 600V. Figure 35, shown the three power diodes connected in power circuit.

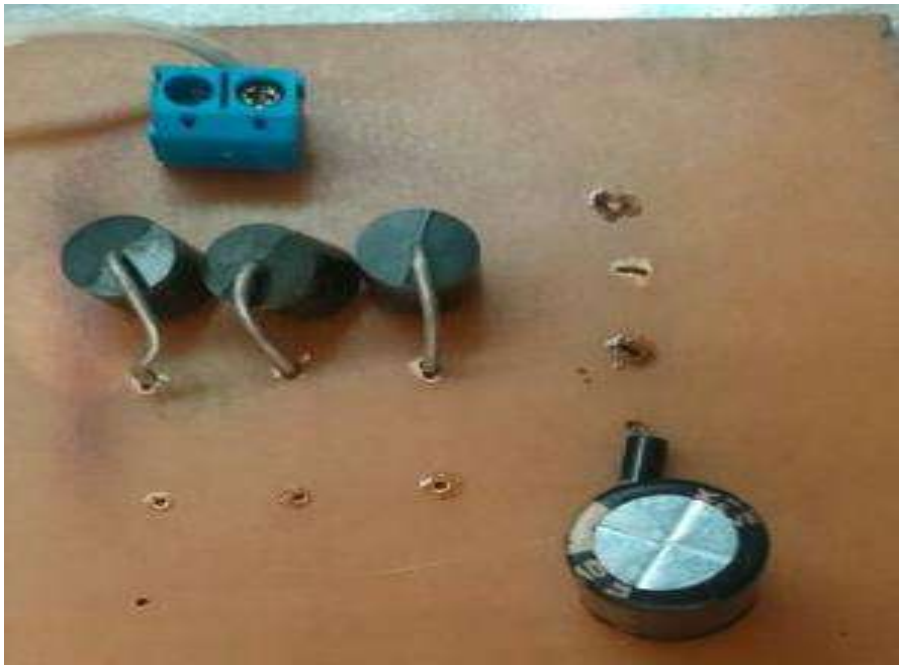

Figure 35: Power Diodes

4.8.4 Power Supplies

When using an inverter, electrical equipment must be isolated from each other. Therefore, four separate power supplies provided to the driver board. The drive assembly connected to the power switch must be powered from a separate power supply to avoid interrupting the current from the device. The diagram of the electrical power supply used is shown in Figure 36.

Figure 36: Power supply [20]

4.8.5 Design of Gate Drive Circuit for IGBT

The FPGA based SPWM signal voltage is about 2V to 3V, but the gate operated voltage is +12V to -12V, which allow the switch to operate at different frequencies. Therefore, gate drive circuit is design to provide required voltages for control the switches of inverter. The HCPL3120 chip is used to provide sufficient gate driver. The schematic diagram of the IGBT gate drive circuit is shown in Figure 37.

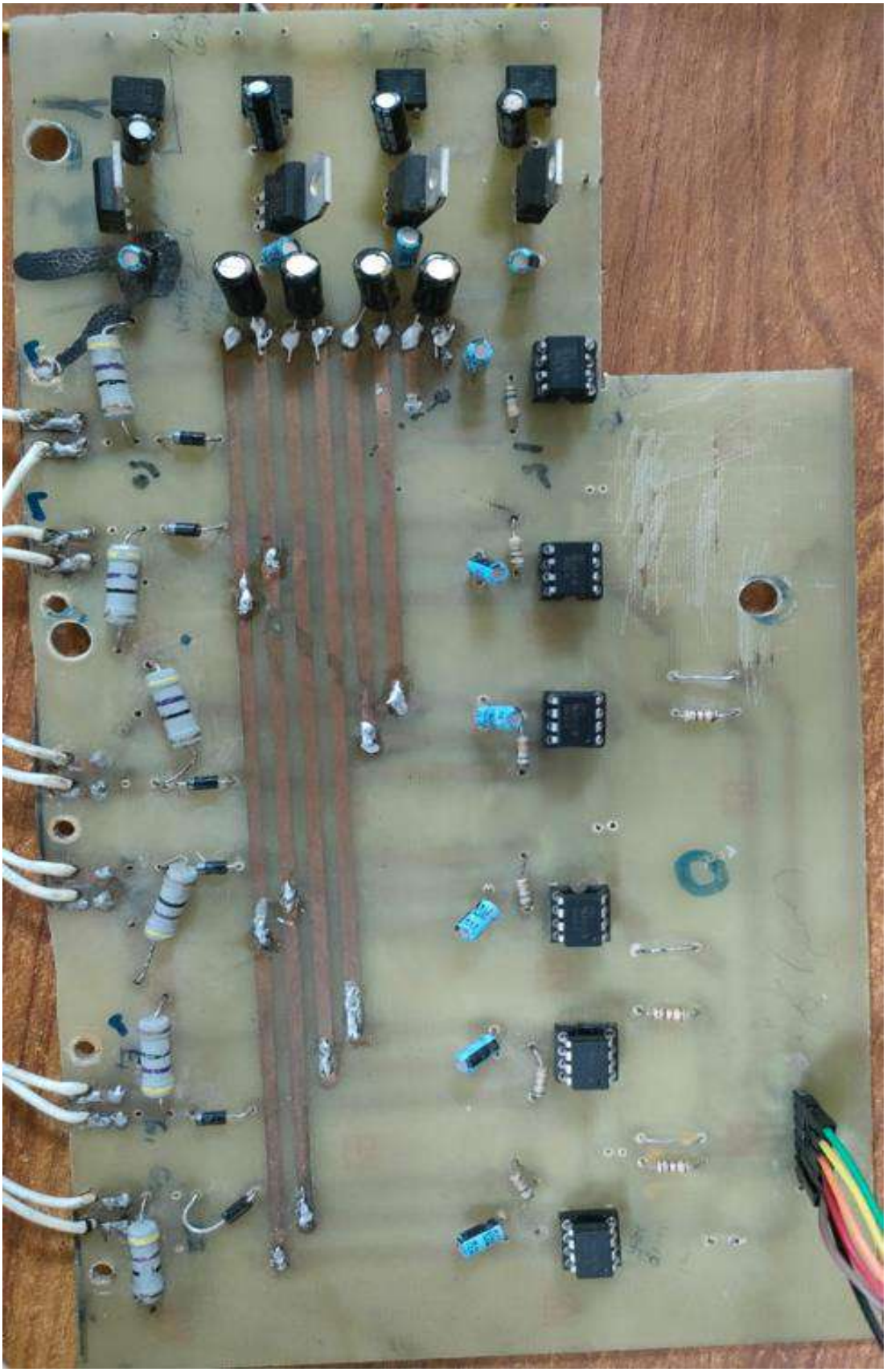

Figure 37: Gate Drive Circuit

The driver opto-isolator IC HCPL 3120 is used to provide optical isolation between the power circuit and controller.

The following reasons highlight the advantages of using the HCPL3120.

1. The maximum input threshold voltage current is 5 mA.
2. 10V–35V power supply voltage
3. 2A is the maximum output current
4. 0.5 second response time
5. A 2500Vrms extraction voltage.

4.8.6 Design the Coupled Inductor (Specifications for proposed inverter)

L1 is 3.3mH and L2 is 6.6mH Switching Frequency is 5 kHz Inverter input is 90V-DC and output is 190V-AC

Step 1: Determine the turns ratio

The turn's ratio is given by the square root of the ratio of the inductance values, i.e.

$$\frac{N2}{N1} = \left(\frac{L2}{L1}\right)$$

$$\frac{N2}{N1} = \sqrt{\frac{6.6mH}{3.3mH}}$$

$$\frac{N2}{N1} = \sqrt{2}$$

$$\frac{N2}{N1} = 1.414$$

Where N1 is the number of turns of the first inductor and N2 is the number of turns of the second inductor.

Step 2: Determine the inductor values

The inductance of each inductor is given by the following equation:

$$L = \frac{(N^2 * \mu * A)}{1}$$

Where N is the number of turns, is the core material's permeability, A is the core's cross-sectional area, and l is the core's length.

Assuming a magnetic core with a permeability of 10000, a cross-sectional area of 1 cm^2, and a length of 4 cm, we can calculate the required number of turns for each inductor as follows:

$$N1 = \sqrt{\frac{3.3mH * 5kHz}{\mu * A}} = 19\ turn$$

$$N2 = \sqrt{\frac{6.6mH * 5kHz}{\mu * A}} = 26\ turn$$

Step 3: Determine the physical size of the inductor

Based on the number of turns, we can estimate the physical size of the inductor using a core with a cross-sectional area of 1 cm^2 and a length of 4 cm. Assuming a wire gauge of 15 AWG, the dimensions of each inductor would be approximately 3.5 cm in diameter and 2.5 cm in height.

Step 4: Determine the inductor core material

Some common core materials for coupled inductors include ferrite, powdered iron, and laminated steel. Ferrite cores are popular for high-frequency applications due to their low losses and high permeability. Powdered iron cores are suitable for high power applications due to their high saturation flux density and low hysteresis losses. Laminated steel cores are often used for low-frequency applications due to their high magnetic permeability. When selecting a core material for a coupled inductor, the core material selection will depend on the following factors:

Operating frequency: The core material should have a high permeability at the operating frequency of the inverter. A high permeability core will increase the inductance value and reduce the number of turns required for the same inductance value, leading to reduced losses.

Core losses: The core material should have low core losses, especially at the operating frequency of the inverter. Core losses are caused by hysteresis and eddy currents in the core material and can lead to reduced efficiency. The core material's loss determines the amount of power lost as heat within the core. A low-loss core material will provide a higher efficiency coupled inductor.

Permeability: The core material's magnetic permeability determines the inductance of the coupled inductor. A high-permeability core material will provide a higher inductance.

Saturation flux density: The core material's saturation flux density determines the maximum magnetic field strength the core can withstand before saturation. To prevent saturation at large currents, use a core material with a high saturation flux density. To prevent core saturation, which can result in higher losses and decreased efficiency, the core material should have a high saturation flux density.

Temperature stability: The core material's temperature stability determines its ability to maintain its magnetic properties at elevated temperatures.

Cost: It is essential to take into account the cost of the core material because it has a big influence on the inductor's total price.

The table 5 Based on these factors, a suitable core material for your application would be a ferrite material, such as N87 or N95, which has a high permeability at the operating frequency of 5kHz, low core losses, high saturation flux density, and is relatively low cost compared to other materials like powder cores or amorphous metal cores.

Table 5: Key parameters for N87 and N95 Ferrite

Key parameters	N87	N95
Permeability	2500+/- 25%	2500+/- 25%
Curie temperature	170°C	150°C
Saturation flux density	450mT	480mT
Remanence	320mT	370mT
Coercivity	4.0A/m	2.5A/m
Temperature coefficient of permeability	0.25%/°C	-0.15%/°C
Frequency Rang	500kHz	200kHz

In summary, to design the coupled inductor for the given Couple Inductor Diode Assisted boost inverter with a 100V DC input, AC output, and a switching frequency of 5 kHz, we would need to use two inductors with values of 3.3mH and 6.6mH, respectively, and a turns ratio of 1.414. Each inductor would require approximately 19 and 26 turns, respectively, and would have a physical size of approximately 3.5 cm in diameter and 2.5 cm in height.

Chapter 5

Components

5.1 FPGA (Field Programmable Gate Array)

A group of logic modules known as adaptable logic modules (ALMs) exist in FPGAs, along with specialized blocks for signal processing and random-access memory (RAM). In order to verify the finished circuits, these programmable blocks are connected in a series [21].

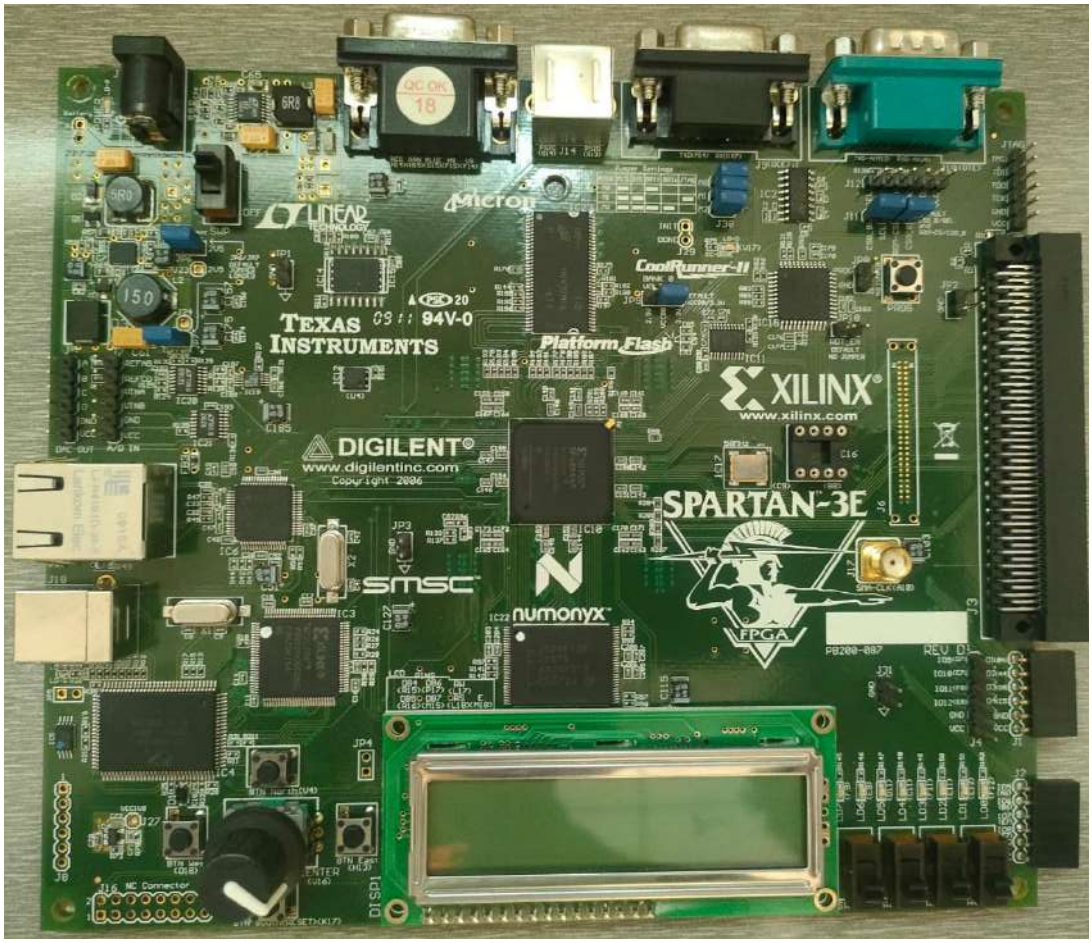

Figure 38: FPGA Spartan 3E

FPGA as shown in the figure 38. The most popular way to design a PWM generator for power conversion applications is to use a field programmable gate array (FPGA). The FPGA design flow eliminates the project's complex and time-consuming floorplan, area and route, check time, and mask/re-rounding because the design patterns are already designed and ready to be embedded in the project[20].

5.2 Gate drive IC

The HCPL-3120 shown in figure 39. This is optocoupler which is consist on GaAsP LEDs. The output of IC circuit is optically paired to the LEDs. These optocouplers widely used in single-phase and three-phase inverter. The output of IC has high operating voltage range which can supplies the necessary driving voltage for the gate controllers. These optocouplers are perfect for directly driving IGBTs rated up to 1200V/100A because of the voltage and current they offer.

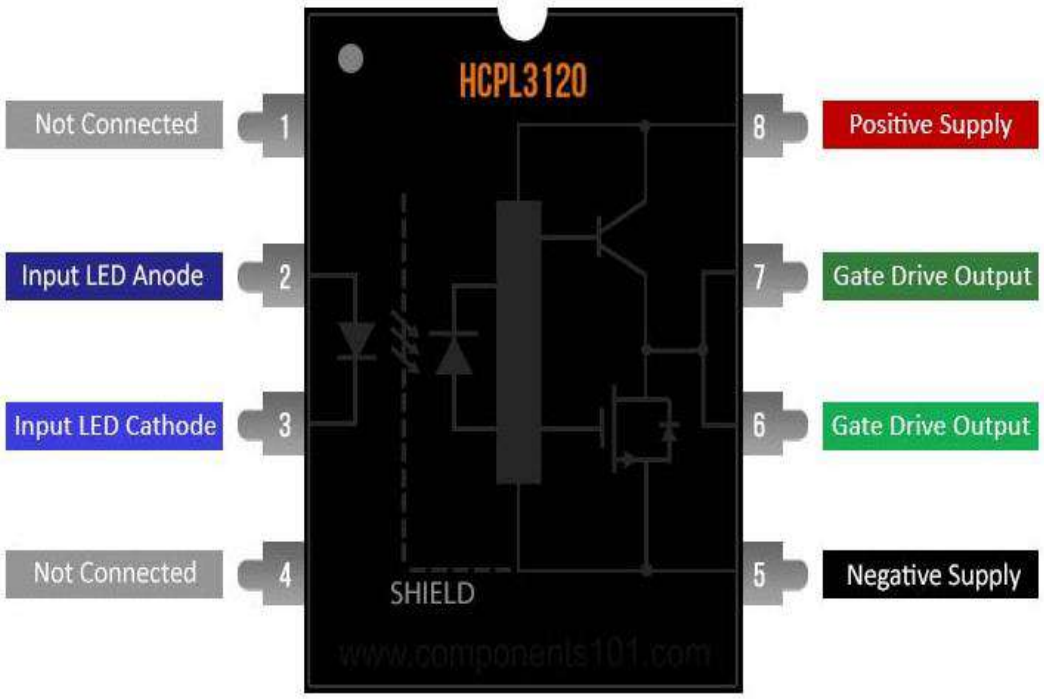

Figure 39: HCPL3120 [21]

5.3 Insulated Gate Bipolar Transistor (IGBT)

Introduced in the late nineteenth century, the gate-isolated bipolar transistor is considered a successful device which shown in figure 40 due to its superior properties. IGBT is a power semiconductor switch, mainly used to control electrical power; There are also many other power applications. IGBTs are called Conductivity Modulated FETs (COMFETs), Insulated Gate Transistors (IGTs), and Bipolar Mode MOSFETs. Soft switching technology has many advantages over hard switching topologies. IGBTs used as soft switching topologies which have the best performance.

Figure 40: IGBTS 2MB1200L 060 [22]

5.4 Single Phase Bridge Rectifier

An electrical device known as a bridge rectifier convert alternating current (AC) into direct current (DC), which only flows in one direction. A full-wave rectifier transforms the complete input waveform into a fixed-polarity (positive or negative) output waveform.

Full wave rectification converts the input waveform's two polarities to pulsed DC (direct current), making the average voltage higher. The bridge configuration must have two diodes and a transformer, or four diodes and an AC source (such as a transformer without a neutral tap) [23]. Single semiconductor diodes, common cathode or common anode dual diodes and quad diode bridges are made. The main application of the rectifier is to obtain DC power from AC power. Rectifier shown figure 41.

Figure 41: Rectifier [24]

5.5 LM7815 Fixed Voltage Regulated IC

The LM7815 is a good voltage regulator IC which shown in figure 42 in the LM78xx series TO-220 package. It has synchronous correction and wide frequency response, easy to use and low cost. Even if the input voltage fluctuates or is stable or higher than 15V, the IC will maintain a constant output voltage of 15V, but the input voltage must not exceed 35V, which is the maximum input voltage limit the IC can handle.

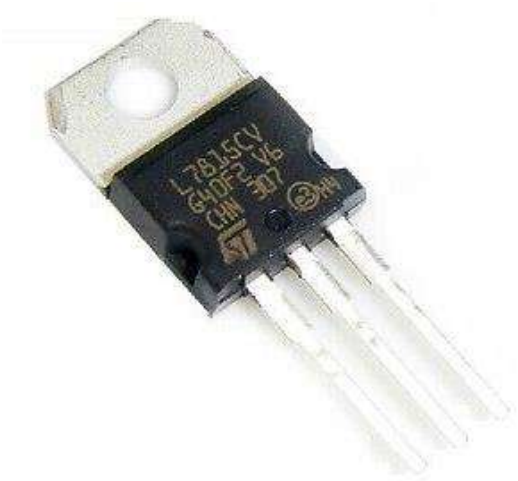

Figure 42: LM7815 [25]

Chapter 6

Results and Discussion

6.1 Final Project View

The main goal of this project is to design and implement an FPGA-based coupled-Inductor diode-assisted three-phase SPWM boost inverter, which aims to efficiently convert DC input power into a high-quality AC output power, utilizing coupled inductors and diode-assisted techniques to achieve improved power conversion efficiency and reduced switching losses. The FPGA-based implementation will enable precise control and modulation of the inverter, which improve power conversion ratio and reduced harmonic distortion.

By implementation FPGA technology, the project seeks to enhance the precision, flexibility, and control of the inverter's operation, enabling seamless integration. The framework is outlined to supply vigorous and solid execution, making it appropriate for different applications such as industrial operations, renewable vitality era frameworks, and smooth uninterruptible control supplies.

The main advantage of this inverter is that FPGA-controlled low-frequency operation minimizes variation, increasing overall efficiency. To reduce ripple and the dv/dt impact a tiny capacitor is connected between the input power source and the inverter. As a result, the system's cost and size may be decreased without compromising its ability to store energy. In addition, we can implement the design in a short time using FPGA.

FPGA is best for designing SPWM generator. Additionally, FPGA-based digital controllers are inexpensive to implement, so they are economically suitable for small inverter designs.

This is the final hardware of the inverter consists of a FPGA SPARTEN 3E board which executing the complex control algorithms and generating precise three phase SPWM signals. This FPGA interfaces with IGBTs to ensure seamless conversion of DC voltage to three-phase sinusoidal output voltages. Fig 39. shown the complete hardware of the proposed inverter.

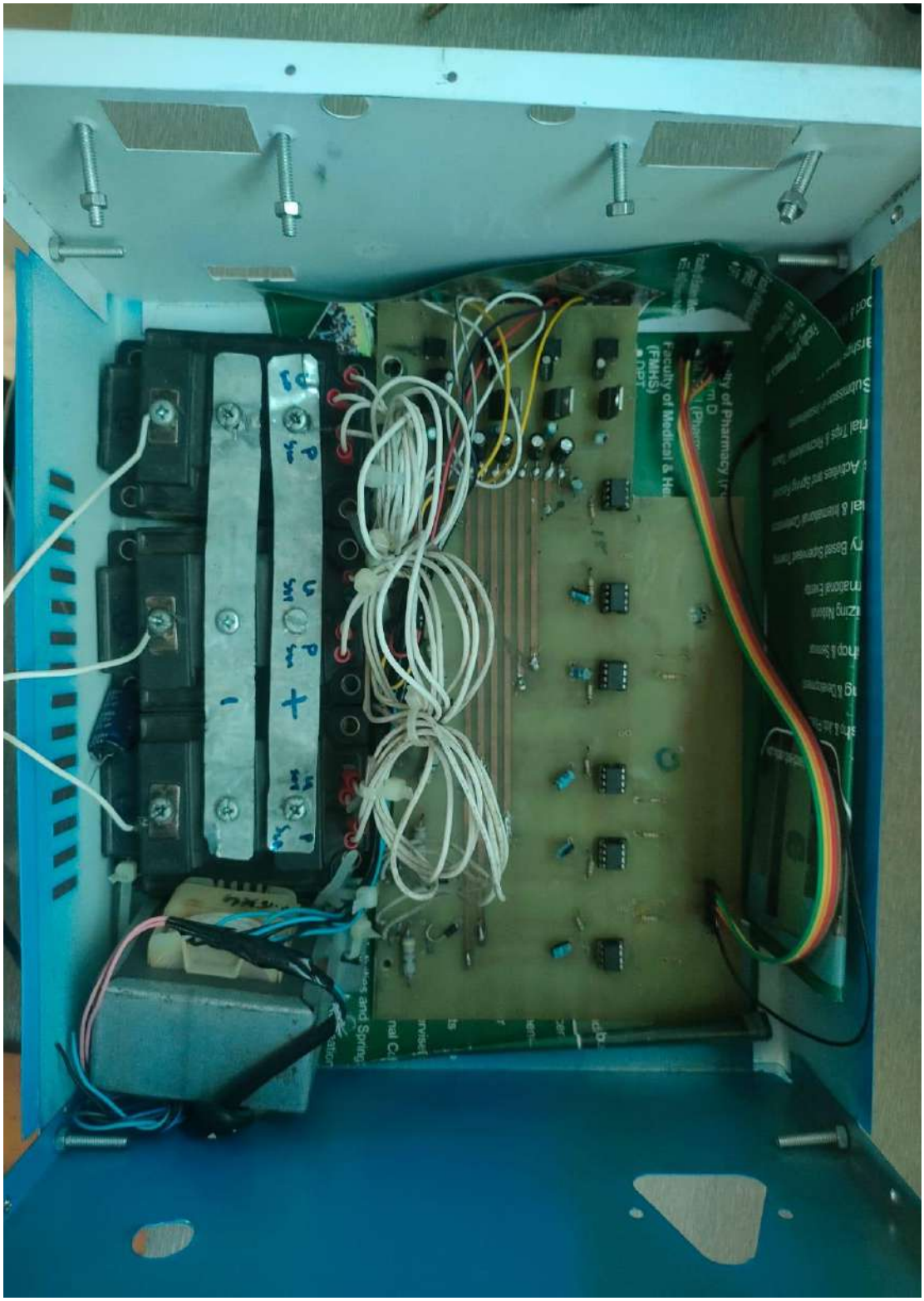

Figure 43: Final Project View

6.2 Three Phase Conventional Inverter MATLAB Simulation

The three-phase inverter is used to provide variable frequency power for industrial applications. Conventional Inverter does not contain any voltage booster system and nor suitable circuit for smooth AC output Voltages. Conventional inverter is shown in Fig 44. Six IGBTs are connected in single stage circuit gating signals is given by SPWM generator. SPWM generator output connected with gates of IGBTs. Three phase SPWM control the switching operation of inverter. In MATLAB oscilloscope is connected for check simulation results of three phase inverter.

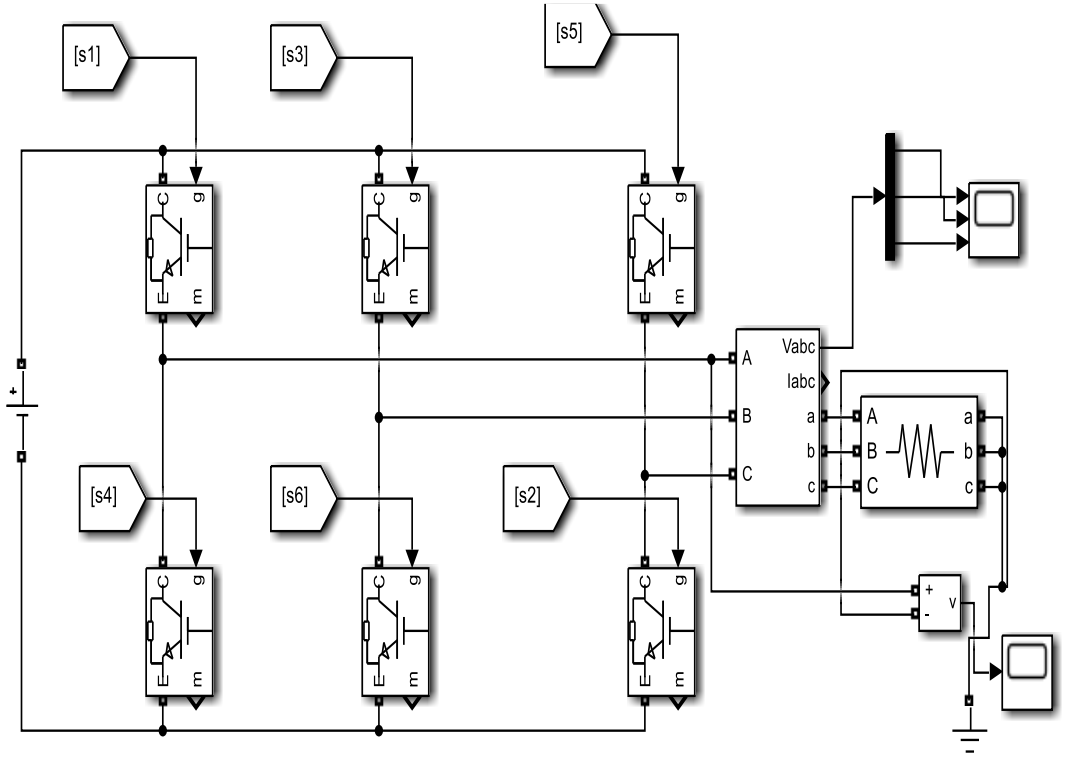

Figure 44: Sinusoidal PWM Three Phase Inverter

6.2.1 Proposed Three Phase Boost Inverter MATLAB Simulation

In the inverter concept, the four diode and a coupled-inductor is connected in such a way that there is no short through and for increasing the average input DC voltage. Figure 45 shows a sinusoidal PWM three-phase boost inverter. Connecting a small capacitor improves the DC-AC connection and helps reduce the dv/dt voltage stress on the power converter. In the inverter concept, high efficiency can be achieved by converting more DC power into AC power while reducing dv/dt voltage stress, overall harmonic distortion, large and expensive components.

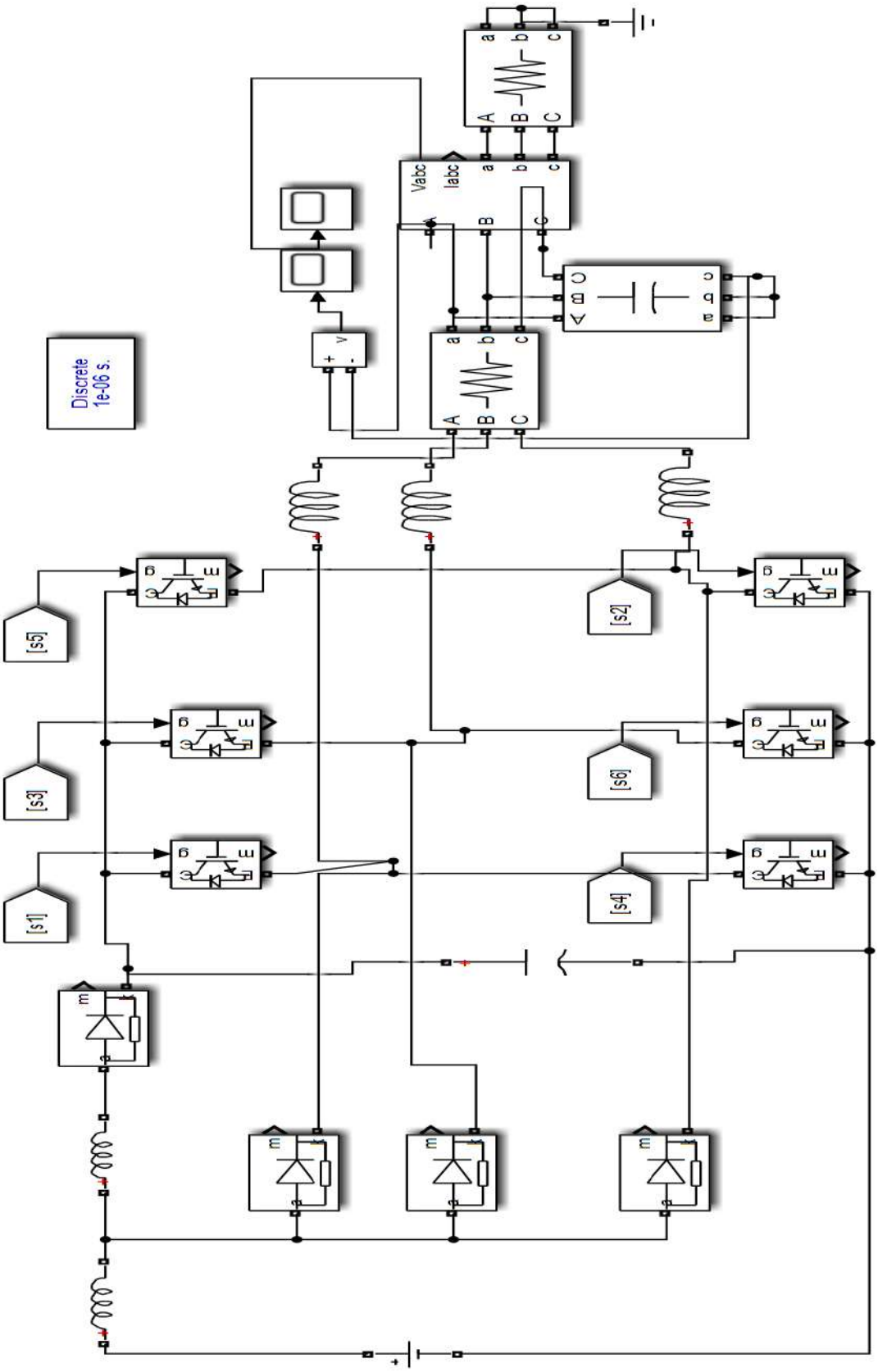

Figure 45: Sinusoidal PWM Three Phase Boost Inverter

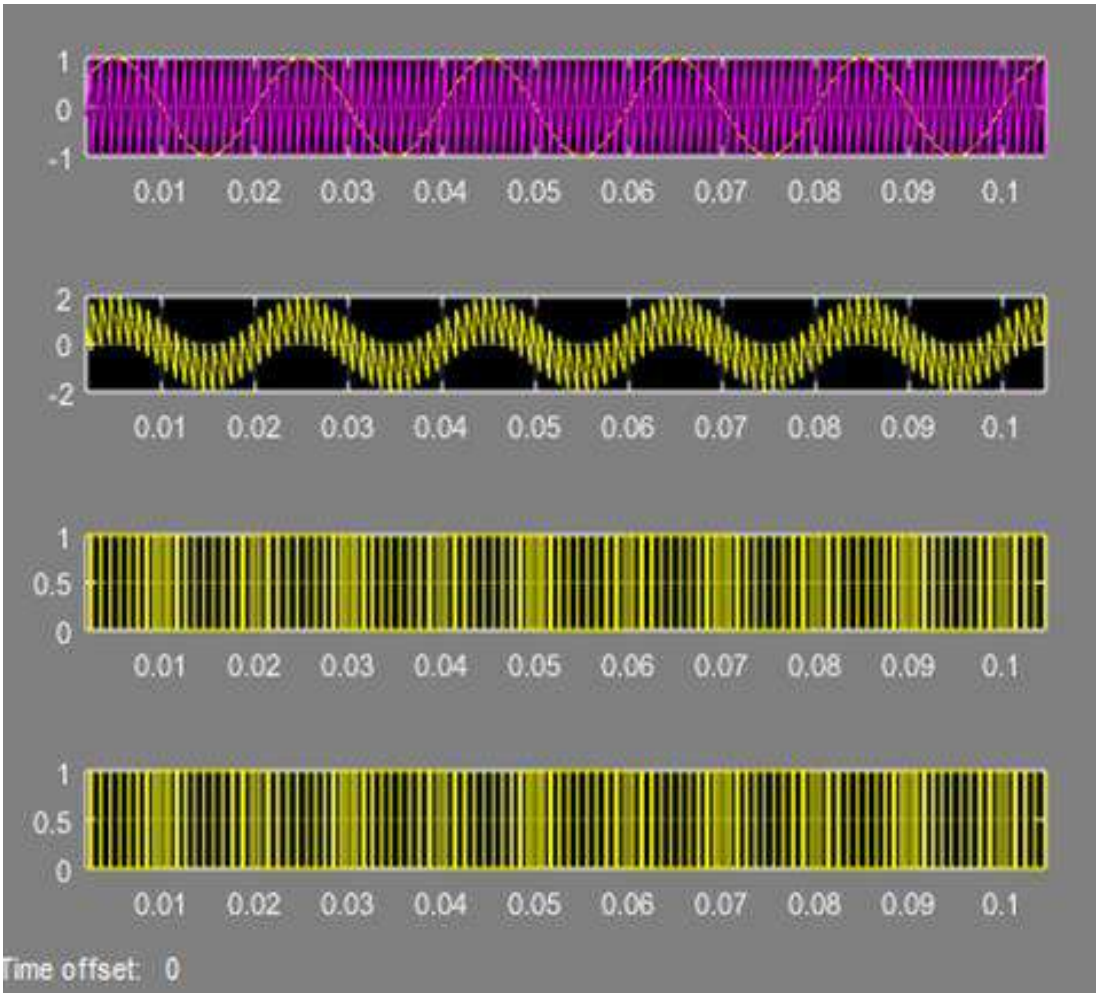

Figure 46: Input signal for both Three Phase proposed boost inverter

6.2.2 Comparison

Comparative analysis of output AC voltages of three phase inverter and proposed Three phase boost inverter is checked with MATLAB simulations. Both inverters is connected with same SPWM input and output observed on oscilloscope in MATLAB simulation show results of both inverter.

Observation of both inverter output voltages show that proposed inverter has less distortion and has better AC output voltages than conventional single stage inverter. Also conversion ratio is very low of conventional three phase inverter as compare proposed single stage three phase boost inverter.

Fig 48. Clearly show that output voltages of conventional three phase inverter has more distortion and harmonics. Output voltages also not smooth its look like quasi square wave it’s not pure sine wave output.

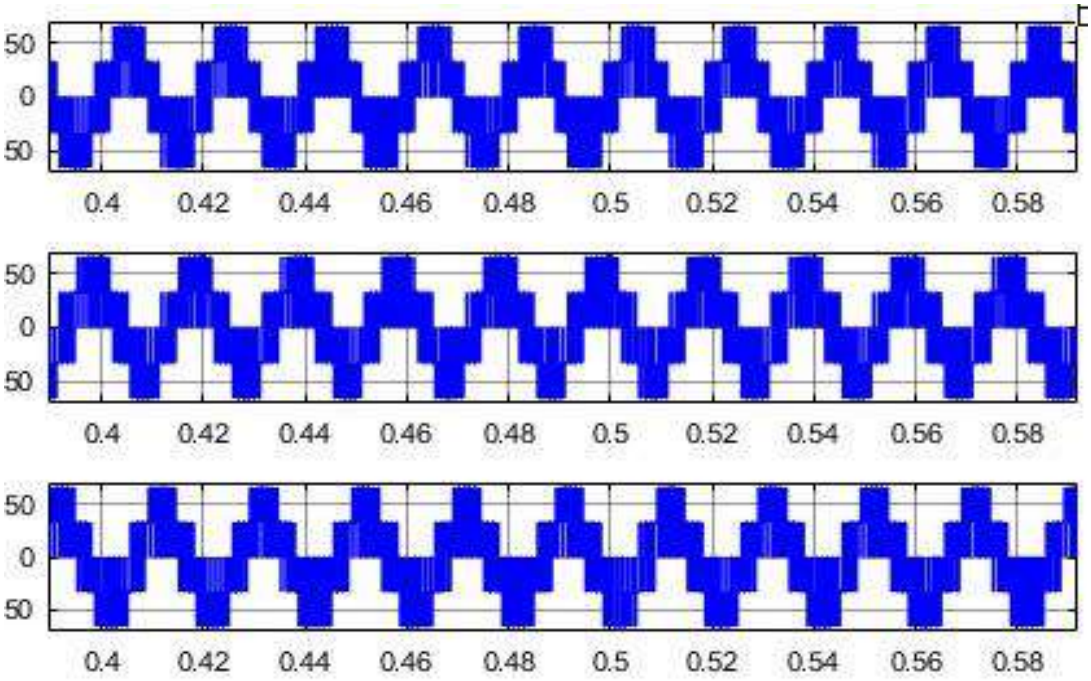

Figure 47: Output Result of Three Phase Conventional Inverter

Output of proposed three phase boost inverter no minor distortion and less harmonics as compare Conventional Inverter.

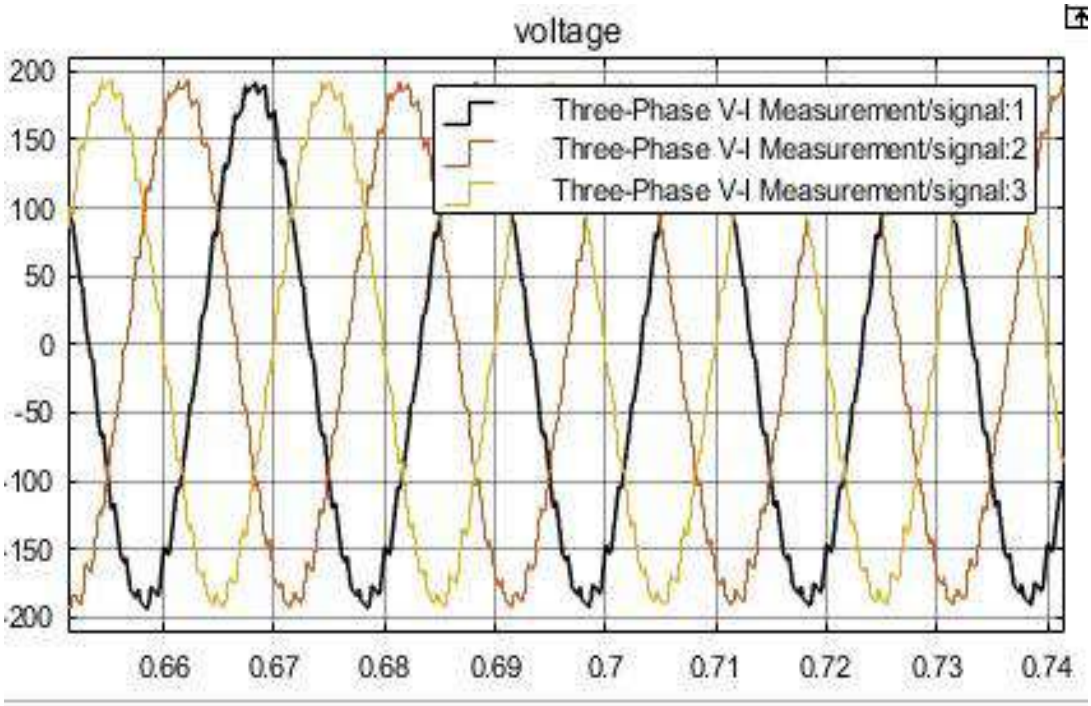

Figure 48: Output Result of Proposed Three Phase Boost Inverter

As it can be seen in Figure 44, that as in the output wave form of proposed Three Phase coupled-inductor Inverter harmonics reduces significantly.

6.3 ModelSim Simulation Results

As SPWM signal generated in MATLAB three sinewave 120 angle shifted with each other compared with triangular wave which produce three phase SPWM signal is same method is implemented in ModelSim using VHDL language it construct a code for generation of SPWM signal which can control switching operation of three Phase inverter. ModelSim Simulation results of SPWM signal generation is shown in Fig 49 and 50.

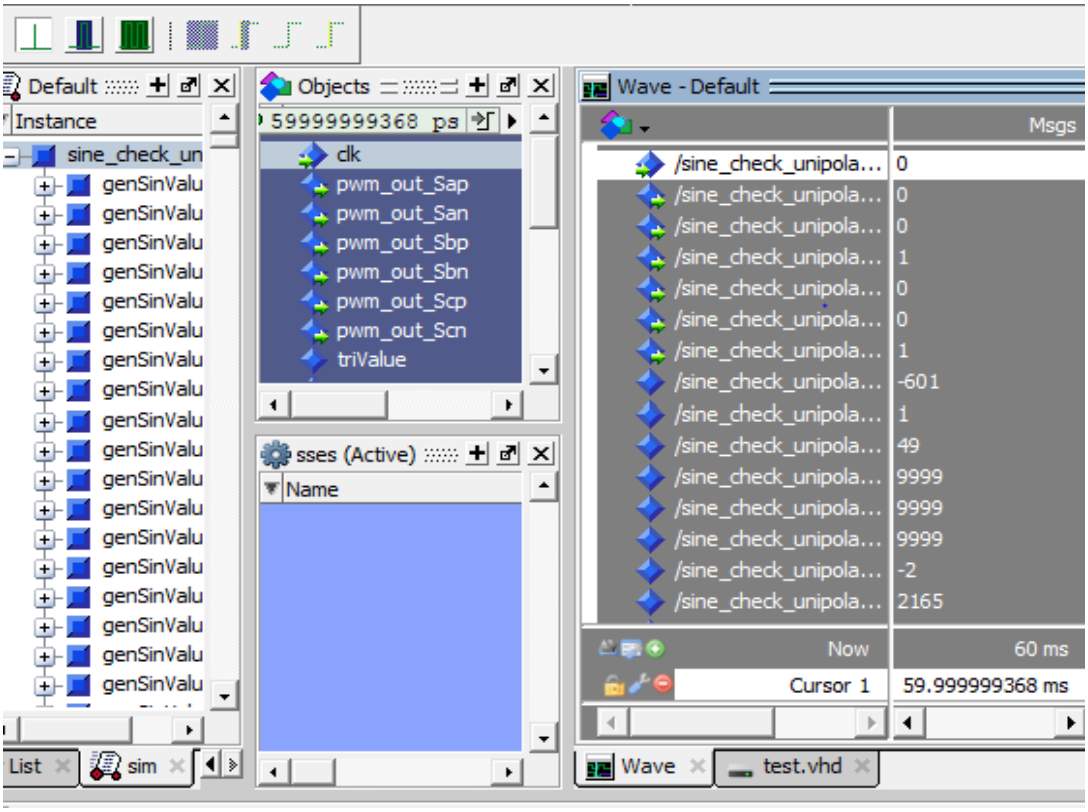

Figure 49: SPWM Wave Generation

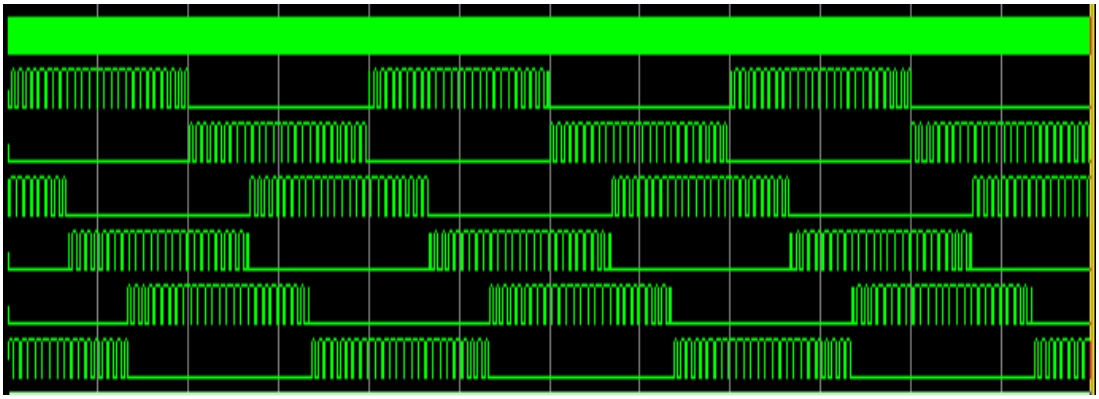

Figure 50: ModelSim simulation of Three Phase SPWM

6.4 FPGA Board SPWM Generation and AC Output Voltage Results on Oscilloscope

Download VHDL programming BIT file into FPGA then selected output pins of FPGA board connected with oscilloscope. Oscilloscope window shown in Fig.51 SPWM signal which operate to switches of proposed three phase inverter.

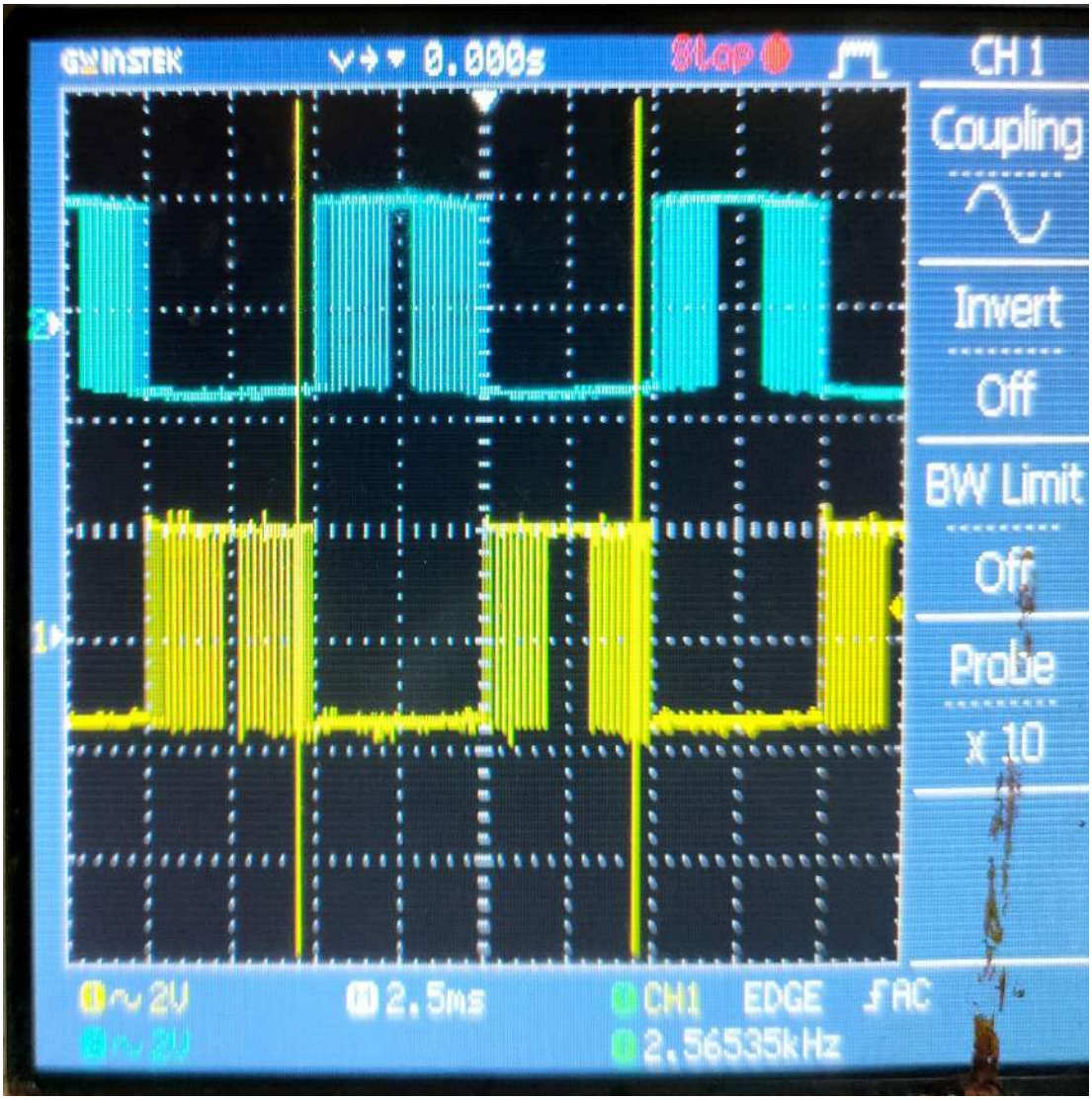

Figure 51: FPGA Board SPWM Wave

After observation of switches control signal result on oscilloscope, FPGA board selected pins connected with IGBTs of three phase inverter input dc supply is given to proposed inverter. Three Phase output voltages is produced by inverter. Three phase voltages verified by connected oscilloscope knobs with the output legs of inverter as shown in Fig 52. Simulation and experimental results are shown in Fig 53-54.

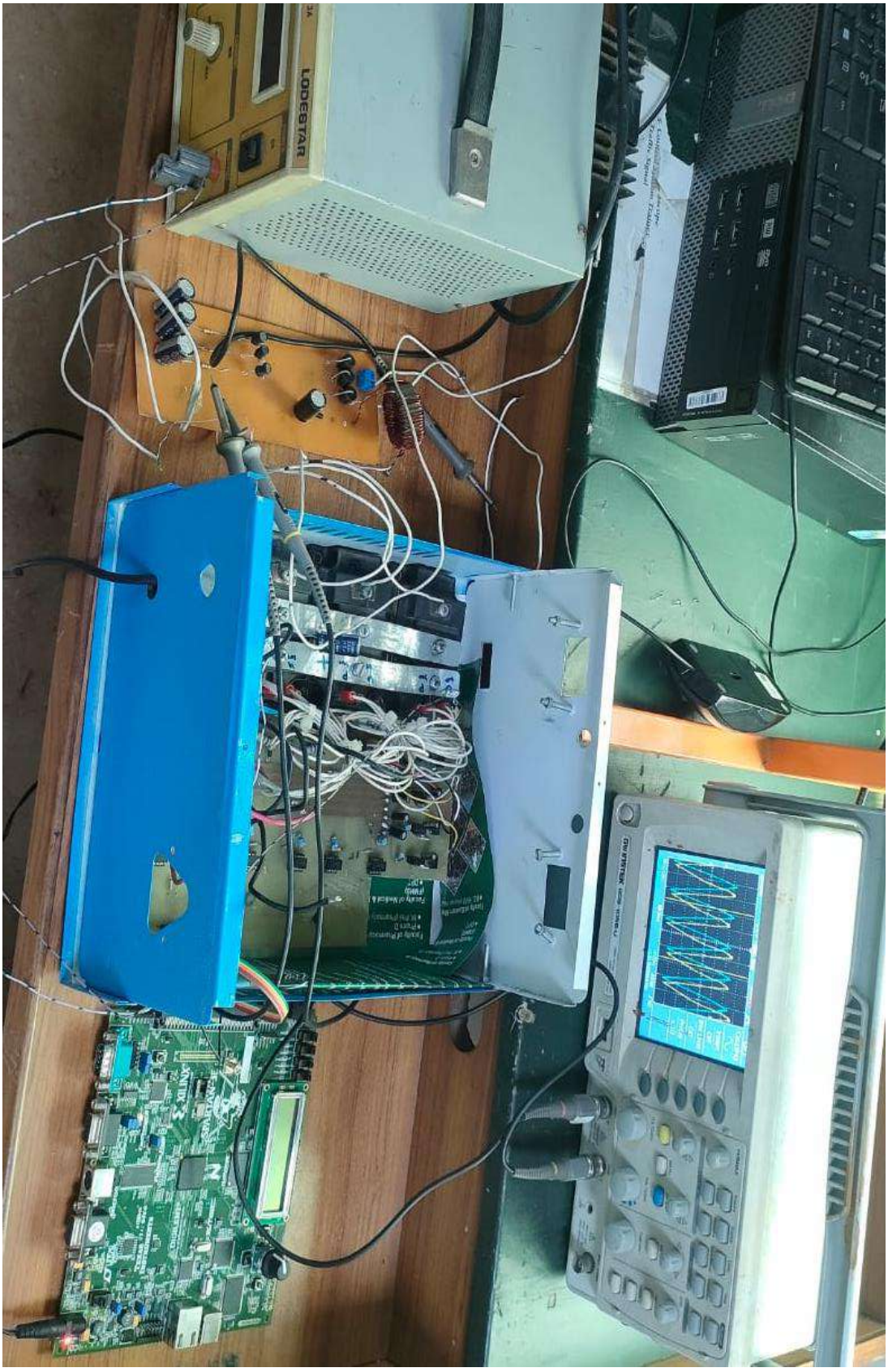

Figure 52: Final project view with Oscilloscope

Table 6: Parameter values used for simulation and experiment

Input Voltage V_{in}	**100 V**
Output Voltage $V_{line,rms}$	190 V
Inductor L_1	3.3 mH
Inductor L_2	6.6 mH
Turns Ratio *n*	$\sqrt{2}$
Capacitor C_1	100 µF
Switching Frequency f_s	5 kHz
Filter Capacitor C_f	86 µF
Filter Inductor L_f	2.4 mH
Resistive Load R_L	20–100 Ω/phase

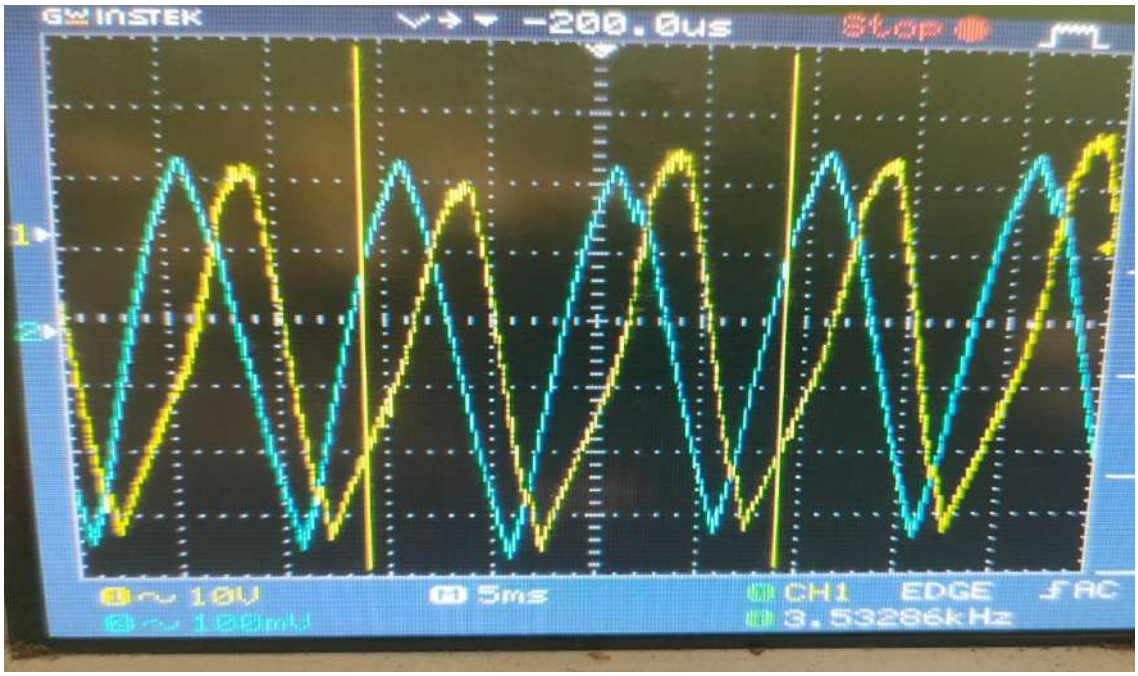

Figure 53: Inverter Output Phase-voltage vph

The hardware results show that the performance of the FPGA-based three-phase SPWM inverter achieves high average DC gain, excellent DC-AC coupling, low stress, power contrast. Lower frequency operation reduces the switching losses, thereby the efficiency of inverter is increased. A smaller value capacitor is used between boost circuit and converter to keep the ripples minimum and voltage stress effect is also negligible. Therefore, the cost and size of system is reduced without compromising on the power handling capacity.

Chapter 7

Conclusion

In the proposed project, we successfully implemented an innovative FPGA-based coupled-inductor diode assisted three-phase SPWM inverter, integrating coupled-inductor and diode assistance. The inverter demonstrates enhanced voltage output quality, reduced losses, and improved efficiency as compared to the traditional inverters. Through FPGA based SPWM, we achieved precise control, ensuring optimal performance and efficient operation. Coupled inductor helps to achieve high gain by selecting appropriate turns ratio. Reverse recovery problem due to diodes is reduced in the presented boost inverter. This problem is alleviated because of leakage inductance and performance of the inverter is improved. Using PWM scheme, it was found that the conversion ratio is low and high dc gain resulted is stress on devices. Therefore, FPGA bases SPWM is introduced to get maximum benefits from the proposed power conversion system. Advantages of this inverter are described below in detail:

Coupled-inductor produced high gain when it is connected with input supply. Turn ratio for inductor was set very low, for which dc input voltage was boosted up-to three times the input DC voltage. By setting higher turns ratio, dc-link voltage could be amplified to a larger value. It was tested that output AC voltages could be easily maintained by just changing modulation index in given [0–1] range, even if the input voltage is not stable around 100V. This property of inverter makes it suitable to work with variable low-voltage dc sources.

Low-frequency based operation maintain the switching losses at lower level, therefore efficiency of the system is higher. A small value capacitor is installed between the boost circuit and inverter to reduce the ripples. The cost and size of the system are reduced without compromising on the power handling capacity.

This solution holds great promise for applications demanding high-quality power conversion in various industries. The proposed inverter topology exhibits excellent performance under different operating conditions, such as changes in input voltage, load variations, and environmental temperature changes. The experimental outcomes demonstrate that the suggested inverter topology achieves a high efficiency. Proposed FPGA based inverter give high gain on full load. The output voltage regulation is achieved with a high accuracy of ±5%, and the total harmonic distortion

(THD) of the output voltage is less than 30%. The project is working fine for the resistive load. FPGA control accuracy higher than all other related microcontrollers therefore non-shoot through switching operation is achieved through FPGA. However, in contrast, CL-DABI capable to convert large power with good quality. In the proposed three-phase inverter, high gain is achieved with higher conversion efficiency, while minimizing the typical drawbacks such as voltage stress, large and costly components, poor power quality, inrush current etc.

7.1 Future Recommendation

- These inverter can be utilized in variable frequency drive application.
- UPS circuit and low-cost solid state frequency charger circuit.
- Automotive applications.
- Battery power systems.
- Consumer electronics

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APPENDEX

Appendix A: FPGA Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.numeric_std.all;
entity sinecheckunipolar is
port (  clk: in  std_logic;
        pwm_out_Sap, pwm_out_San: out std_logic;
        pwm_out_Sbp, pwm_out_Sbn: out std_logic;
        pwm_out_Scp, pwm_out_Scn: out std_logic );
end sine_check_unipolar;
architecture spwm_3phase of sine_check_unipolar is
  signal triValue: integer range -1251 to 1251 := 0;
  signal countSin: integer range 0 to 101:= 0;
signal sinIndex_phase1, sinIndex_phase2, sinIndex_phase3: integer range 0 to 10000
:= 0;
signal sinValue_phase1, sinValue_phase2, sinValue_phase3: integer;
  signal sinTable_phase1, sinTable_phase2, sinTable_phase3: sintab;
begin
  genSinValues_phase1: -- Generate the sine value table for phase 1
  for idx in 0 to 9999 generate
     constant x: real := SIN(real(idx)*real(2)*math_pi/real(10000));
     constant xn: signed(17 downto 0) := to_signed(integer(x*real(1250)),18);
end generate;
genSinValues_phase2: -- Generate the sine value table for phase 2
```

```
    for idx in 0 to 9999 generate
    constant x: real := SIN(real(idx - 6666)*real(2)*math_pi/real(10000)); -- Phase shift of 120 degrees (10000/3 = 3333.33)
    constant xn: signed(17 downto 0) := to_signed(integer(x*real(1250)),18);
    end generate;
  genSinValues_phase3: -- Generate the sine value table for phase 3
    for idx in 0 to 9999 generate
    constant x: real := SIN(real(idx - 3333)*real(2)*math_pi/real(10000)); -- Phase shift of 240 degrees (2*10000/3 = 6666.66)
    constant xn: signed(17 downto 0) := to_signed(integer(x*real(1250)),18);
    end generate;
incSineVal: process (sinIndex_phase1, sinIndex_phase2, sinIndex_phase3) -- Each time the sine index changes, fetch a new value from the table
  begin
    sinValue_phase1 <= to_integer(sinTable_phase1(sinIndex_phase1));
    sinValue_phase2 <= to_integer(sinTable_phase2(sinIndex_phase2));
    sinValue_phase3 <= to_integer(sinTable_phase3(sinIndex_phase3));
  end process incSineVal;
  indexCount: process (clk)
  begin
    if rising_edge(clk) then
      -- Increment the triangle wave signal
      triValue <= triValue + triDir;
      -- If at peak amplitude,
      if triValue >= 1250 then
        triDir <= -1;
      elsif triValue <= -1250 then
```

```
      triDir <= 1;
    end if;
    -- Increment count value
    countSin <= countSin + 1;
    -- If time to change sine value
    if countSin >= 99 then
      countSin <= 0;
   -- Increment the sine table indices for each phase
      sinIndex_phase1 <= sinIndex_phase1 + 1;
      sinIndex_phase2 <= sinIndex_phase2 + 1;
      sinIndex_phase3 <= sinIndex_phase3 + 1;
      if sinIndex_phase1 >= 9999 then
        sinIndex_phase1 <= 0;
      end if;
      if sinIndex_phase2 >= 9999 then
        sinIndex_phase2 <= 0;
      end if;
      if sinIndex_phase3 >= 9999 then
        sinIndex_phase3 <= 0;
      end if;
    end if;
  end if;
 end process indexCount;
 -- Compare Value of Sine Wave with Triangle Wave on each clock edge for each phase
 pwmOutput_phase1: process (clk)
```

```
 begin
   if rising_edge(clk) then
if sinIndex_phase1 <= 4979 then
    if sinValue_phase1 > triValue then
      pwm_out_Sap <= '1';
      pwm_out_San <= '0';
    else
      pwm_out_Sap <= '0';
      pwm_out_San <= '0';
    end if;
else
    if sinValue_phase1 > triValue then
      pwm_out_Sap <= '0';
      pwm_out_San <= '0';
    else
      pwm_out_Sap <= '0';
    pwm_out_San <= '1';
    end if;
end if;
   end if;
 end process pwmOutput_phase1;
 pwmOutput_phase2: process (clk)
 begin
   if rising_edge(clk) then
   if sinIndex_phase2 <= 1657 then
   if sinValue_phase2 > triValue then
```

```
        pwm_out_Sbp <= '1';
        pwm_out_Sbn <= '0';
      else
        pwm_out_Sbp <= '0';
        pwm_out_Sbn <= '0';
      end if;
elsif sinIndex_phase2 >= 1657 and sinIndex_phase2<=6667 then

      if sinValue_phase2 > triValue then
        pwm_out_Sbp <= '0';
        pwm_out_Sbn <= '0';
      else
        pwm_out_Sbp <= '0';
        pwm_out_Sbn <= '1';
      end if;

elsif sinIndex_phase2 >= 6678 and sinIndex_phase2 <=9999 then
      if sinValue_phase2 > triValue then
        pwm_out_Sbp <= '1';
        pwm_out_Sbn <= '0';
      else
        pwm_out_Sbp <= '0';
        pwm_out_Sbn <= '0';
      end if;
end if;
    end if;
```

```
  end process pwmOutput_phase2;
  pwmOutput_phase3: process (clk)
  begin
    if rising_edge(clk) then
  if  sinIndex_phase3  <= 3323 and sinIndex_phase3>=0 then
      if sinValue_phase3 > triValue then
        pwm_out_Scp <= '0';
        pwm_out_Scn <= '0';
      else
        pwm_out_Scp <= '0';
        pwm_out_Scn <= '1';
      end if;
elsif   sinIndex_phase3 >= 3334 and sinIndex_phase3<=8324 then
      if sinValue_phase3 > triValue then
        pwm_out_Scp <= '1';
        pwm_out_Scn <= '0';
      else
        pwm_out_Scp <= '0';
        pwm_out_Scn <= '0';
      end if;
      end if;
      end if;
  end process pwmOutput_phase3;
end architecture spwm_3phase;
```

Appendix B: IGBTs Data Sheet

IGBT MODULE (L series)

■ Features

G High Speed Switching

O Low Saturation Voltage

O Voltage Drive

■ Applications

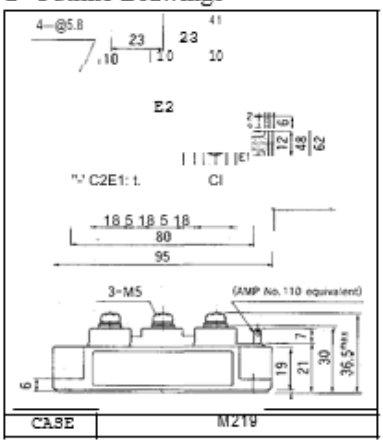
O Inverter for Motor Drive

G AC and DC Servo Drive Amplifier

G Uninterruptible Power Supply

G Industrial Machines, such as Welding Machines

■ Outline Drawings

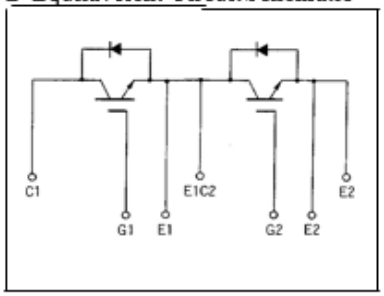


■ Maximum Ratings and Characteristics

G Absolute Maximum Ratings

Items		Symbols	Ratings	Units
Collector-Emitter Voltage		VcEs	600	V
Gate-Emitter Voltage		VGES	+20	V
Collector Current	Continuous	IC	200	A
	1ms	Ic pulse	400	
	Continuous	—Ic	200	
	1ms	—Ic pulse	400	
Max. Power Dissipation		Pc	800	W
Operating Temperature		T	+150	°C
Storage Temperature		Tstu	—40 to +125	°C
Net. Weight			340	g
Isolation Voltage	AC. Imin.	Visoi	2500	V
Screw Torque		Mounting *1 Terminals *1	35 35	kg' cm

■ Equilavelent Circuit Schematic



G Electrical Characteristics (Tj=25°C)

Items	Symbols	Test Conditions	Min.	Typ.	Max.	Units
Zero Gate Voltage Collecter Current	ICEs	Vor—OV Vcz=600V Ti=25°C			2.0	mA
Gate-E mitter Leackage Current	IsEs	Vcz=0V Vca-+ 20V			200	nA
Gate-Emitter Threshold Voltage	Vol it⊙	Vcc=20V Ie 200mA	30		6.0	V
Collecter-Emitter Saturation Voltage	VcEpap	Vcr=15V Ic=200A		2.7	3.5	V
Input Capacitance	Cies	VGE=0V Vcz=10V f=1MHz		19000		pF
Output Capacitance	Coes					
Reverse Transfer Capacitance	Cres					
Turn-on Time *2		Vcc=300V Ic=200A Ver— + SV Rc—9.1U		0.6	0.8	s
	ton			0.4	0.6	
Turn-offTime'3	tr			0.7	1.0	
	toff			0.2	0.35	
Diode Forward On-Voltage	tf Vf	Ir=200A Vsr=0V			2.5	V
Reverse Recovery Time	trr	Ir=200A —di/dt=600A/is VIE=—10V			300	ns

Appendix C: IC Data Sheet

Electrical characteristics of IC 7815

Output Voltage				5V			12V			15V			Units
Input Voltage (unless otherwise noted)				10V			19V			23V			
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_J = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA	T_J = 25°C		3	50		4	120		4	150	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
			0°C ≤ T_J ≤ +125°C			50			120			150	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 1A	T_J = 25°C			50			120			150	mV
			ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
			0°C ≤ T_J ≤ +125°C			25			60			75	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	T_J = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ T_J ≤ +125°C				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	T_J = 25°C			8			8			8	mA
			0°C ≤ T_J ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		T_J = 25°C, I_O ≤ 1A				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN}≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 500 mA, 0°C ≤ T_J ≤ +125°C				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN}≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A =25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, T_J = 25°C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA 0°C ≤ T_J ≤ +125°C	62			55			54			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ

Output Voltage			5V			12V			15V			Units
Input Voltage (unless otherwise noted)			10V			19V			23V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Short-Circuit Current	Tj = 25˚C		2.1			1.5			1.2		A
	Peak Output Current	Tj = 25˚C		2.4			2.4			2.4		A
	Average TC of V_{OUT}	0˚C ≤ Tj ≤ +125˚C, I_O = 5 mA		0.6			1.5			1.8		mV/˚C
V_{IN}	Input Voltage Required to Maintain Line Regulation	Tj = 25˚C, I_O ≤ 1A		7.5		14.6			17.7			V