HARDWARE REALIZATION OF MULTILEVEL INVERTER

A thesis submitted by

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Submitted in the partial fulfillment of the requirements for the degree ofBachelor of Engineering in Electrical Engineering

Department of Electrical Engineering

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CERTIFICATE

This is to certify that **–Hardware Realization of Multilevel Inverter"** is submitted in partial fulfillment of the requirement for the degree of Bachelor of Engineering in Electrical Engineering by the following students:

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MOTIVATION

In the realm of industrial power systems, the demand for higher voltage and power levels has been steadily increasing to meet the growing energy needs of modern industries. Traditional two-level inverters have limitations when it comes to high-voltage applications due to increased switching losses and lower voltage resolution, resulting in lower power quality and efficiency. To overcome these limitations and cater to the requirements of industrial applications, multilevel inverters have emerged as a promising solution. Multilevel inverters offer significant advantages, including improved voltage waveform quality, reduced harmonics, lower switching losses, and increased efficiency. These benefits make them well-suited for various industrial processes, such as motor drives, renewable energy integration, and high-voltage power transmission. Our project fall into one of the SDG's created by the UN as it will help in Multilevel inverters can improve energy efficiency and facilitate the integration of renewable energy sources into industrial grids. By enhancing power conversion efficiency, the project aligns with the goal of ensuring access to affordable, reliable, sustainable, and modern energy for all.

ACKNOWLEDGEMENT

I bear witness that none is worthy of worship but ALLAH, the One alone, without partner, and I bear witness that Muhammad is His servant and Messenger.

We would like to express our deepest appreciation to all those who provided us the possibility to complete this project. A special gratitude we give to our final year project supervisor Dr.Engr.Shahryar Shafique IQRA National University Peshawar whose contribution in stimulating suggestions and encouragement helped us to coordinate our final year project.

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ABSTRACT

This paper presents single phase nine level cascaded H-Bridge Multilevel Inverter using SPWM control technique. The conventional inverter has many limitations for high voltage and high power applications. Multilevel Inverter becomes very popular for high voltage and high power applications. There are 3 types of Multilevel Inverters named as Diode clamped Multilevel Inverters, Flying capacitor Multilevel Inverters and Cascaded H-bridge Multilevel Inverters. Cascaded H-bridge topology is used in this paper with SPWM control technique. This topology uses less number of switches as compared with conventional topologies, where it reduces the complexity and overall size of the system which in turn reduces the harmonics and cost of the entire system. All simulations are done in Matlab/Simulink. A low pass LC filter is also designed and simulated for single phase Multilevel Inverter in this paper. LC filter is used for minimization of harmonics at the output side of the inverter. By the use of above said topology and filter the output has less THD‘s (Total Harmonic Distortion) as compared to other multilevel inverters

ABBREVIATIONS

MLI: Multi-Level Inverter

THD: Total Harmonics Distortions

MW: Mega Watt

NPCI: Neutral Point-Clamped Inverter

CMLI: Cascaded Multi-Level Inverter

DC: Direct Current

AC: Alternative Current

FFT: Fast Fourier Transform

LSF: Low Switching Frequency

SDC: Separated DC Sources

PWM: Pulse Width Modulation

SPWM: Sinusoidal Pulse with Modulation

SVPWM: Space Vector Pulse Width Modulation**C:** Capacitor

L: Inductor

R: Resistor

DCs: Duty Cycles

SWM: Square Wave Modulations

MOSFET'S: Metal Oxide Field Effect Transistors

PCB: Printed Circuit Board

PD: Phase Disposition

POD: Phase Opposition Disposition

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CHAPTER-1

INTRODUCTION

Multilevel inverters have been under research and development for more than three decades and have found successful industrial applications. However, this is still a technology under development, and many new contributions and new commercial topologies have been reported in the last few years. The aim of this dissertation is to groupand review recent contributions, in order to establish the current state of the art and trendsof the technology to provide readers with a comprehensive and insightful review of wheremultilevel converter technology stands and is heading. This chapter first presents a brief overview of well-established multilevel inverters strongly oriented to their current state inindustrial applications and then centers the discussion on the new multilevel inverters thathave made their way into the industry. Multilevel inverters have been attracting increasing interest recently the main reasons are; increased power ratings, improved harmonic performance, and reduced electromagnetic interference (EMI) emission that can be archived with multiple dc levels that are synthesis of the output voltage waveform. In particular multilevel inverters have abundant demand in applications such as medium voltage industrial drives, electric vehicles, and grid connected photovoltaic systems.

Multilevel power conversion technology is a very rapidly growing area of power Electronics with good potential for further development. The most attractive application of this technology is in the medium-to-high-voltage range, motor drives, power distribution, and power conditioning applications. In recent years, industry demands power in the megawatt level. Controlled ac drives in the Megawatt (MW) range are usuallyconnected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family ofmultilevel inverters has emerged as the solution for working

with higher voltage levels. The developments in power electronics and semiconductor technology have triggered the improvements in power electronic systems. So, different circuit configurations namely multilevel inverters have become popular and considerable interest by researcher are given on them. The output voltage waveforms in multilevel inverters can be generated at low switching frequencies with low distortion and high frequency. For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly

[1] [2] [3]. As a result, a Multi-Level power converter structure has been introduced as an alternative in high power and medium voltage situations such as Laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. The concept of multilevel inverters has been introduced since 1975. The cascaded multilevel inverter was first introduced in 1975. Separate DC-sourced full bridge cells were placed in series to synthesize a staircase AC output voltage. The term multilevel began with the three level converter. Subsequently, several multilevel converter topologies have been developed. In 1981, diode-clamped multilevel inverter also called the Neutral-Point Clamped (NPC) inverter schemes were proposed [5]. In 1992, capacitor-clamped (or flying capacitor) multilevel inverters, and in 1996, cascaded multilevel inverters were proposed [1]. Although the cascade multilevel inverter was invented earlier, its application did not prevail until the mid-1990s.The advancements in the field of power electronics and microelectronics made it possible to reduce the magnitude of harmonics with multilevel inverters, in which the number of levels of the inverters are increased rather than increasing the size of the filters. The performance of multilevel inverters enhances as the number of levels of the inverter increases.

1.1 OBJECTIVES

In general multilevel inverter can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The main advantages of this approach are summarized as follows:

- They can generate output voltages with extremely low distortion and lower (dv/dt).
- They draw input current with very low distortion.
- They can operate with a lower switching frequency (LSF).
- Their efficiency is high (>98%) because of the minimum switching frequency.
- They are suitable for medium to high power applications.

Multilevel inversion is a power conversion strategy in which the output voltage is obtained in steps thus bringing the output closer to a sine wave and reduces the total harmonic distortion (THD). Various circuit configurations namely diode clamped, flying capacitor and cascaded, etc., have been proposed [11].

1.2 CONCEPT OF MULTILEVEL INVERTERS

Multilevel inverter includes an array of power semiconductor devices and capacitors voltage sources, the output of which generates voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages to obtain high voltage at the output, while the power semiconductors have to withstand only reduced voltages.

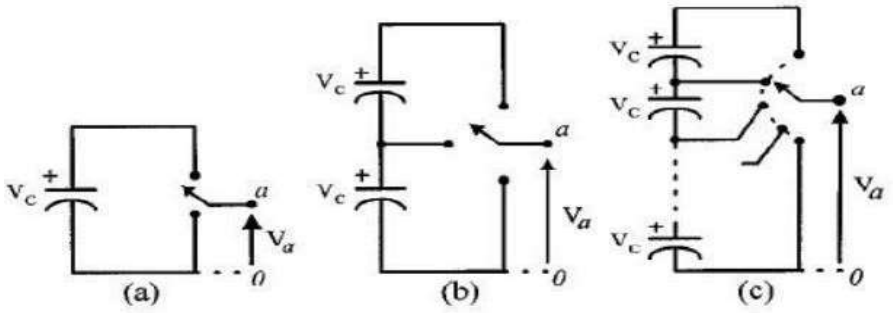


Fig 1.1: Multi-Level concepts a) two level b) three level c) nine level

Fig.1.1 shows a schematic diagram of Multi-level concepts a) two level. b) Three level. c) Nine level, one phase leg of inverters with different numbers of levels, for which the action of power semiconductors is represented by an ideal switch with several positions. Form Fig.1.1, we can observe a two level inverter generates an output voltage with two values (levels) with respect to negative terminal of the capacitor.

While the three level inverter generates three voltages, and a nine-level inverter generates a nine level output voltages. In all this cases devices are not arranged in series but they arearranged in such way that, they gain the capability to generate such kind of voltages. Herein, we should remember one important thing i.e. as the number of steps increases in the output waveforms; harmonic content comes down [10]. Thus power quality of such waveforms will increase drastically. However, in order to generate step kind of waveforms in output side, different Multilevel based archetypes are successfully built and verified. But general principle of multilevel inverters is the synthesis of the ac voltage from several different voltage levels on the dc bus. As the number of voltage levels on the input dc sideincreases, the output voltage adds more steps [5-10], which approach the sinusoidal wave.

1.3 MULTI-LEVEL TOPOLOGIES

The basic three types of multilevel topologies used are:

i. Diode clamped
ii. Flying capacitors
iii. Cascaded H-bridge

1.3.1 Diode Clamped Topology

Fig 1.2 shows n-level diode clamped Multi-Level Inverter. The diode clamped multilevel inverter uses capacitors in series to divide up the dc bus voltages into a set of voltage level. To produce n levels of the phase voltage, an n level diode clamp inverter needs (n- 1) capacitor on the dc bus.

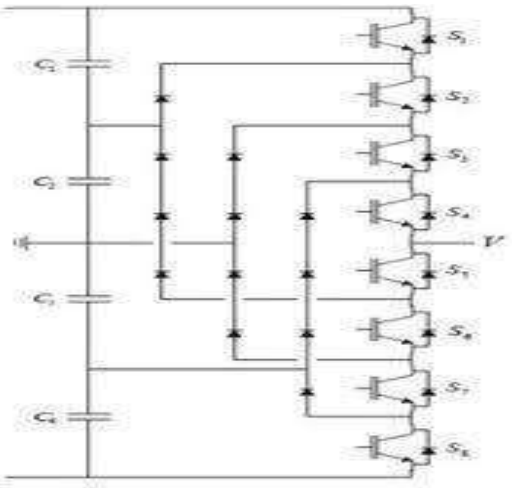


Fig 1.2: n-level diode clamped Multi-Level Inverter

1.3.2 FLYING CAPACITORS

Fig 1.3 shows n-level Flying capacitor Multi-Level Inverter. It uses ladder structures of dcside capacitors where the voltage on each capacitor differs from that of the next capacitor. To generate n-level staircase output voltage, (n-1) capacitors in the dc bus are needed. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output wave.

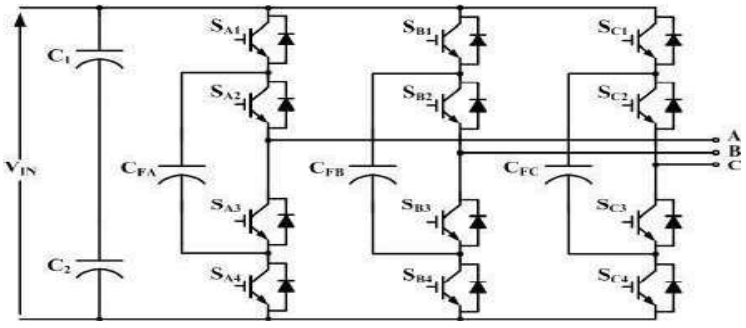


Fig 1.3: n-level Flying capacitor Multi-Level Inverter

1.3.3 CASCADED H-BRIDGE

Fig 1.4 shows n-level Cascaded H-bridge Multi-Level Inverter. This inverter is nothing but the series connection of single connection of single phase inverters with separate dc sources. This inverter can be avoiding the extra clamping diodes or voltage balancing capacitors.

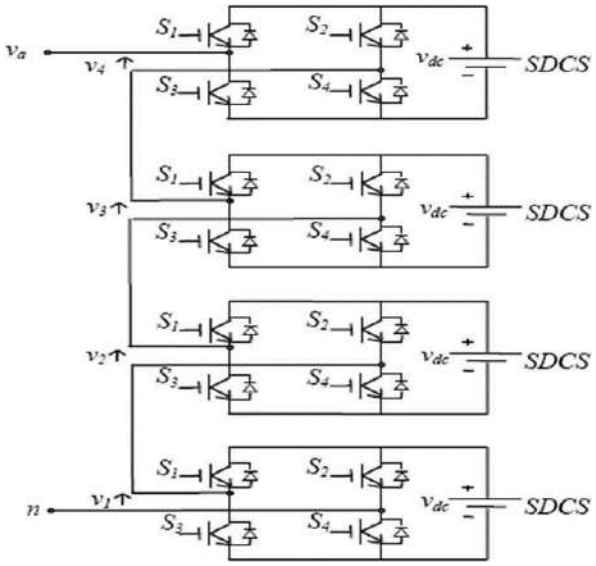


Fig 1.4: n-level Cascaded H-bridge Multi-Level Inverter

CHAPTER-2

LITERATURE REVIEW

2.1 OVERVIEW OF CASCADE H-BRIDGE TOPOLOGY

Cascaded H-Bridge configuration has recently become very popular in high-power AC supplies and adjustable-speed drive applications [4]. A cascade multilevel inverter consistsof a series of H-bridge (single-phase full bridge) inverter units. Each H-bridge unit has itsown dc source. Each SDC (separate D.C. source) is associated with a single phase

Full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Fig. 2.1 shows a single phase structure of a cascaded H-bridge inverter with separate D.C. sources. Through different combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs, +Vdc, -Vdc and zero. To obtain +Vdc switches S1 and S4 are turned on. On turning on S2 and S3 together we get the output –Vdc. On turning the switches S1 and S2 together or S3 and S4 together or S1, S2, S3, S4 simultaneously we get the output 0. The AC outputs of different full- bridge converters are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. In this topology, the number of output-phase voltage levels is defined by M= 2N+1, where ‗M' is the no of levels and ‗N' is the numberof DC sources. So, for an example the output phase voltage of nine level inverter is given by

$$M= 2N+1 \qquad 2.1$$

$$Van= Va1+Va2+Va3+Va4 \qquad 2.2$$

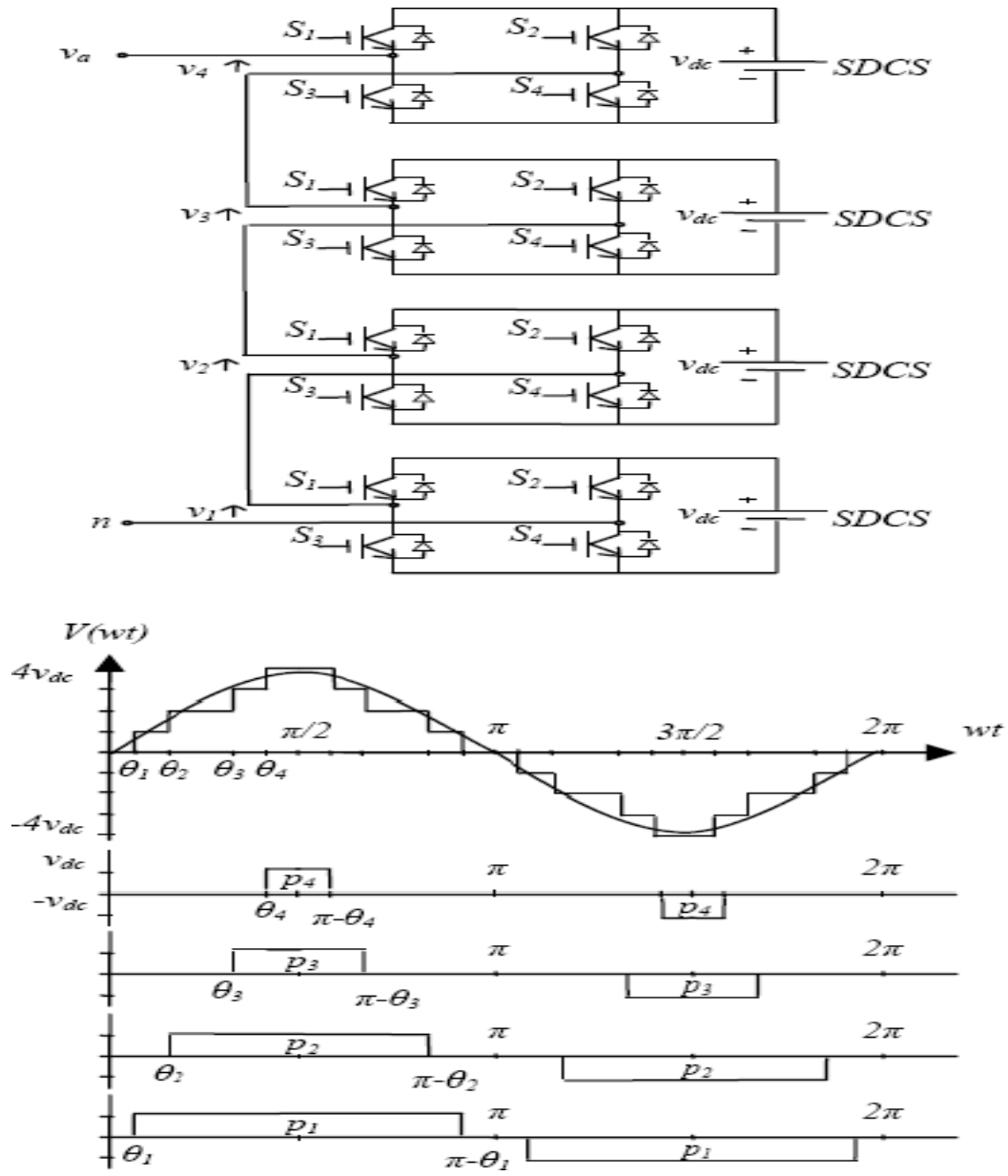


Fig 2.1: Single Phase Structure of a Cascaded H-bridge Inverters

From the single phase structure of a cascaded H-bridge inverter as shown in Fig. 2.1 above, we can make the three level, five level, seven level and nine level inverters without using any type of modulation technique, and by using the same mathematical relation M=2N+1.

2.2 COMPARISON OF DIFFERENT TOPOLOGIES

The utilization of electrical energy was easy and straight forward production of power & its utilization was a linear process but now a day‘s power system one of the

complex networks in the world with invention of new techniques of power control and equipment which has better energy efficiency and reliable control techniques with fast and smart switching [1,3].Before few decade For the operation of electric equipment‘s switching of electric power was either through manually or through electromechanical switches but due to fast response, accuracy and high range the power electronics and solid state controllers and converters has been using Worldwide and in last twodecided their uses increases very rapidly With the help of multi-level inverter we can get the output nearly to sinusoidal voltage waveforms by combining many isolated voltage levels[2].

The summary of comparison of different topologies are presented in Table 2.1.

Table 2.1: Comparison between different topologies of multilevel inverter

Topologies	**Diode Clamped**	**Fly Back**	**Cascaded H-Bridge**
Advantages	Simple Control	Real Power Control	Least number of components
	High efficiency	Reactive Power Control	Number of Voltage levels is same
Disadvantages	More number of clamping diodes according to levels	Complex Control according to levels	Separate DC Sourcesare required

2.3 CONTROL TECHNIQUE

There are many control techniques which is applicable for cascade multilevel inverter aswell as other‘s multilevel inverter like fly back, diode clamped.

- Pulse Width Modulation (PWM)
- Sinusoidal pulse width modulation (SPWM)
- Space-vector pulse width modulation (SVPWM).

Pulse Width Modulation (PWM) technique represent the generation of constant amplitude pulse with the help of modulating the pulse duration by Modulating the duty cycle[6].The reference signal desire, signal output maybe sinusoidal or square wave, while the carrier signal is either a saw tooth or triangular wave at a frequency significantly greaterthan the Reference[] Sinusoidal pulse width modulation technique multiple shows the numbers of output pulse per half cycle and pulses for different width of Individual pulse Varied in Proportion to the amplitude of a sine wave evaluated at center of the same pulse.

2.3.1 Sinusoidal Pulse Width Modulation (SPWM) for multilevel Inverter

SPWM for Multilevel Inverter is based on classic two level SPWM with triangular carrierand sinusoidal reference waveform. Only difference between two level SPWM and multilevel SPWM is, numbers of carriers are used in multilevel SPWM .For _*m*‘ level inverter _*m*-1‘ carrier are used. Interaction of particular carrier and reference is used to generate gating signal for particular complementary pair of switches in diode clamped or capacitor-clamped inverter, or particular cell in multi-cell inverter.

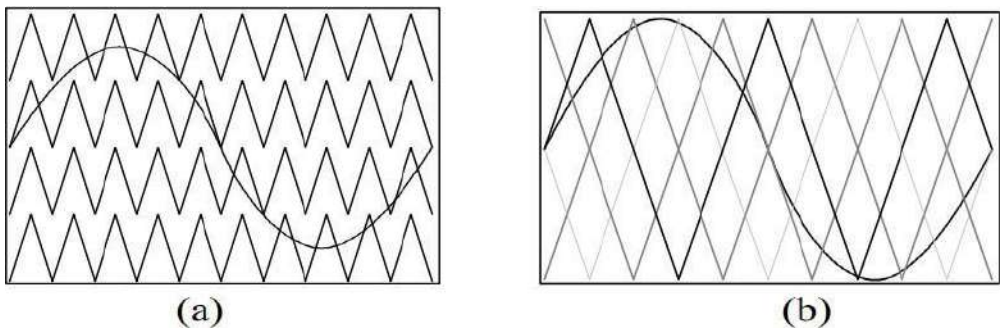


Fig 2.2: (a) vertically shifted carriers. (b) Horizontally shifted carriers

Carriers used in multilevel inverter may be vertically shifted or horizontally shifted as shown in Fig 2.2 (a), (b). Advantage of horizontally shifted carriers scheme is that, each modules are switched on and off with a constant number of times by period, independentlyof magnitude of generated voltage. But vertically shifted carrier scheme can be more easilyimplemented on any digital controller [12].

2.3.2 Implementation of SPWM Technique

Digital implementation SPWM technique is based on classical SPWM technique with carriers and reference sine waveform. Only difference between them is, in digital SPWM a sine table consisting of values of sine waveform sampled at certain frequency is used. Asresult reference wave form in digital SPWM represents a sample and hold waveform of sine wave forms. This sampling of sine waveform comes in two variants; a) Symmetrical sampling, b) Asymmetrical sampling.

In symmetrical sampling, as shown in Fig. 2.3, reference sine waveform is sampled at only positive peak of the carrier waveform and sample is held constant for the complete carrier period. This introduces the distortion in modulating signal and phase shift between modulating signal and fundamental component of output voltage. Here sampling frequency is equal to carrier frequency. The phase shift is given by $\pi \div m_f$, where

$$m_f = f_c \div f_m \qquad 2.3$$

fc= Carrier frequency.

fm = Reference Sine wave frequency.

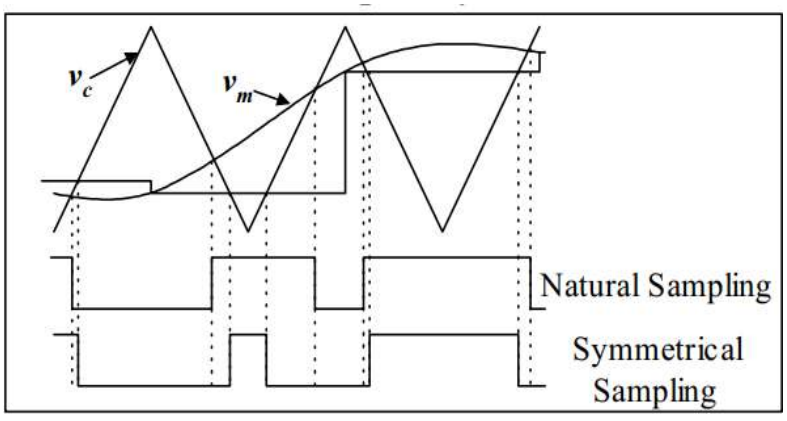


Fig 2.3: Natural sampling, Symmetrical Sampling

In asymmetrical sampling, the reference signal is sampled at positive as well as negative peak of carrier frequency and held constant for half the carrier period. Here sampling frequency is twice the carrier frequency. Asymmetrical sampling is the preferred method, since each switching edge is the result of new sample and give better performance as shownin Fig. 2.4. The phase shift is by $\pi \div 2m_f$.

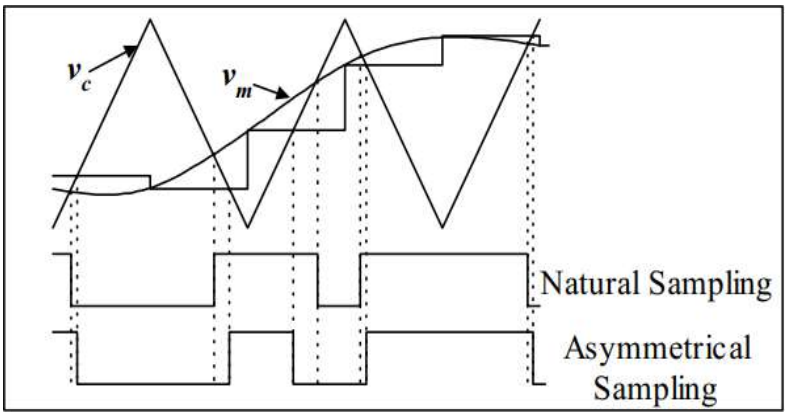


Fig 2.4: Natural sampling, asymmetrical sampling

CHAPTER-3

DESIGN AND SIMULATION RESULTS OF PROPOSED PROJECT

3.1 BLOCK DIAGRAM OF PROPOSED PROJECT

Fig.3.1 shows the block diagram of 9-level cascaded H-bridge multilevel inverter. FourH- Bridges are used with separate DC-sources and also a control circuit which produces pulses.

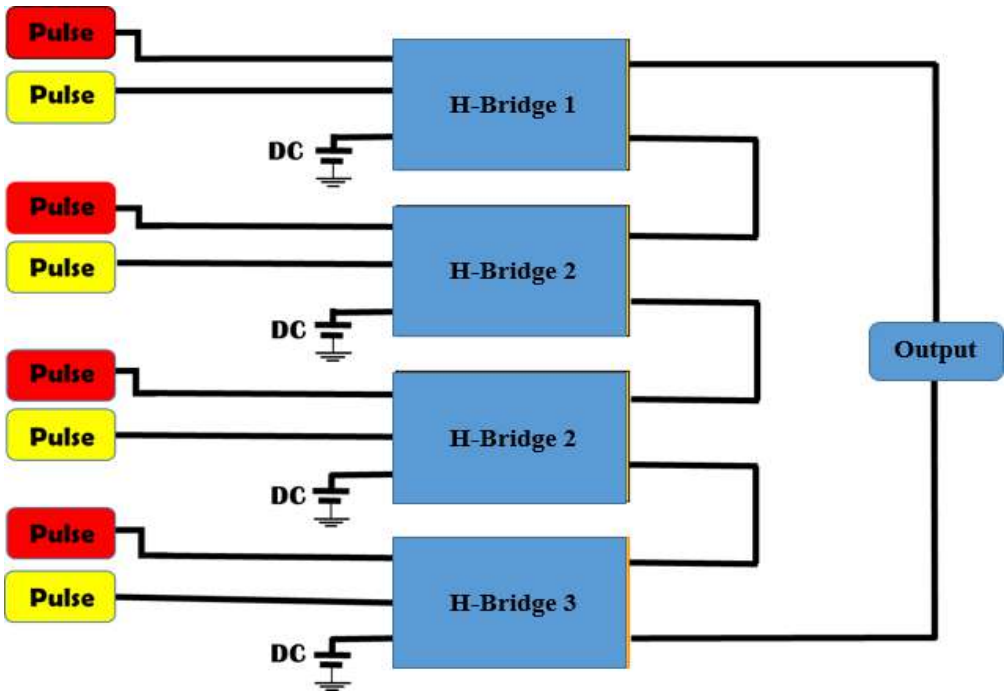


Fig 3.1: Block Diagram of 9-level cascaded H-bridge multilevel inverter

3.2 CIRCUIT DIAGRAM OF PROPOSED PROJECT

Fig. 3.2 shows the complete circuit diagram of 9-level cascaded H-bridge multilevel inverter. This is designed on Simulink MATLAB.

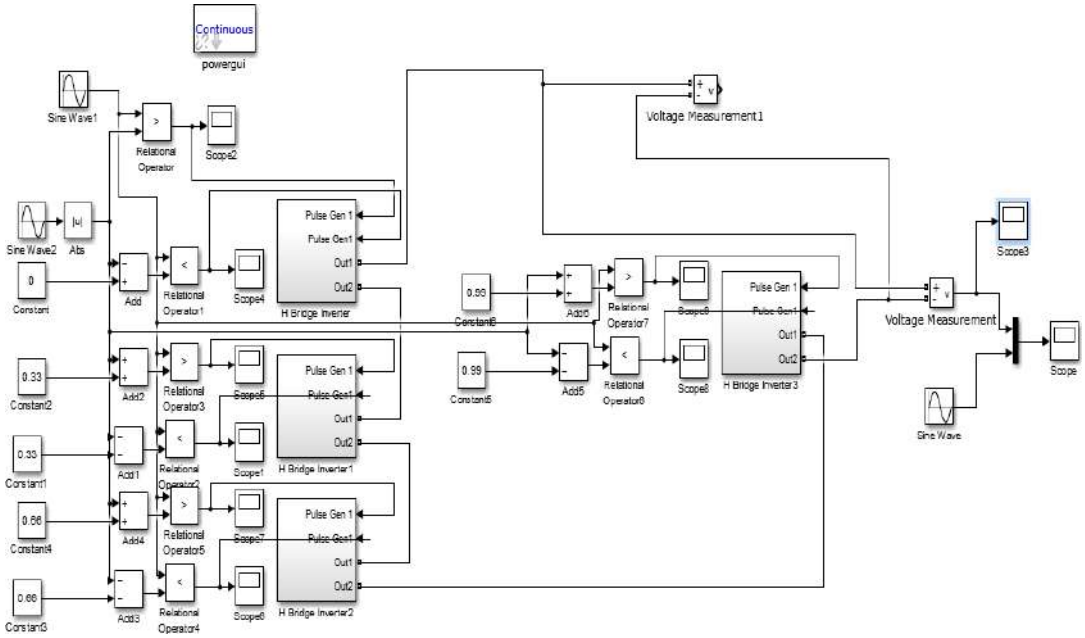


Fig 3.2: Circuit Diagram of 9-level cascaded H-bridge multilevel inverter

3.3 TIMING DIAGRAM OF SWITCHES

Fig. 3.3 shows the Timing Diagram of switches. It explains the duty cycle of each switch.

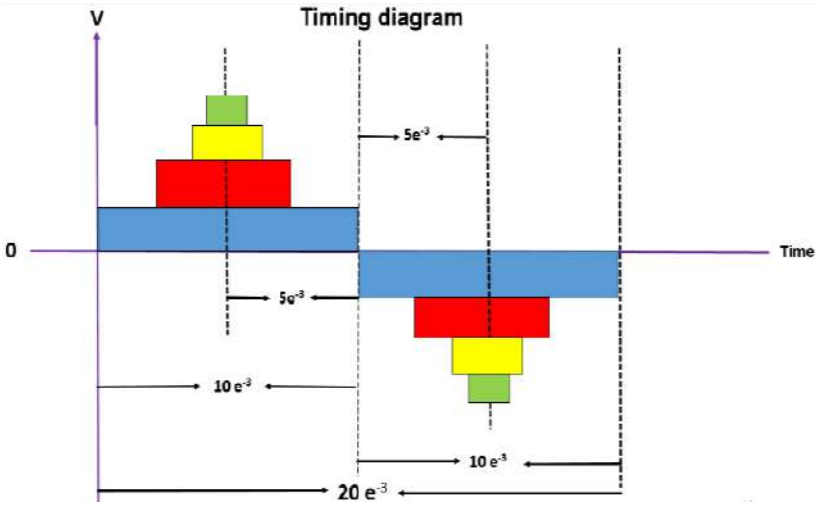


Fig 3.3: Timing Diagram of switches

3.4 SIMULATION RESULTS AND OBSERVATIONS

Fig. 3.4 shows the simulation result of 9-level cascaded H-bridge multilevel inverter. The simulation is done in Simulink MATLAB.

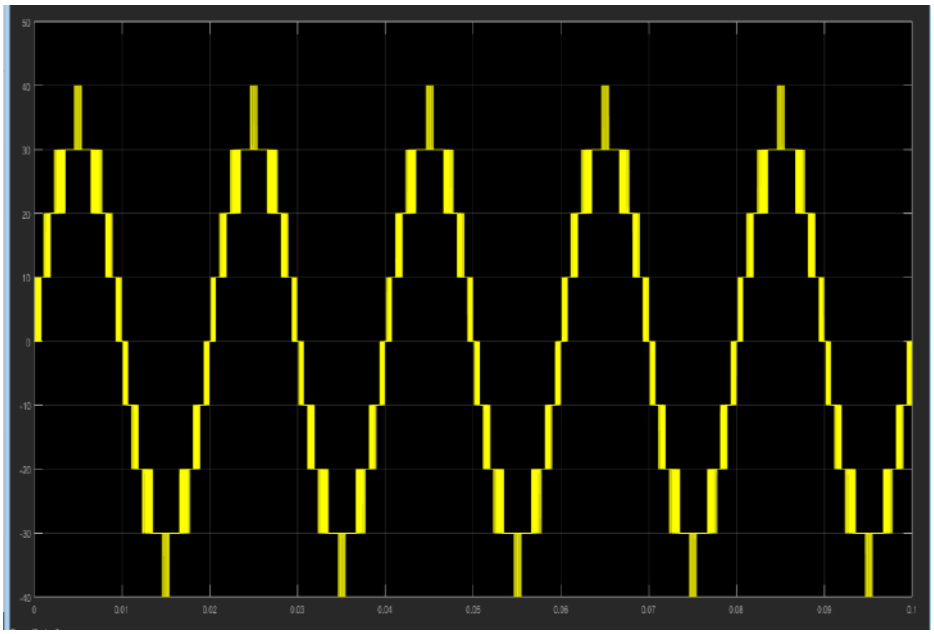


Fig 3.4: Simulation Result of 9-level cascaded H-bridge multilevel inverter

3.5 THD % OF 9-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

Fig 3.5 shows the THD % of 9-level cascaded H-bridge multilevel inverter without filter and found to be 15.11%.

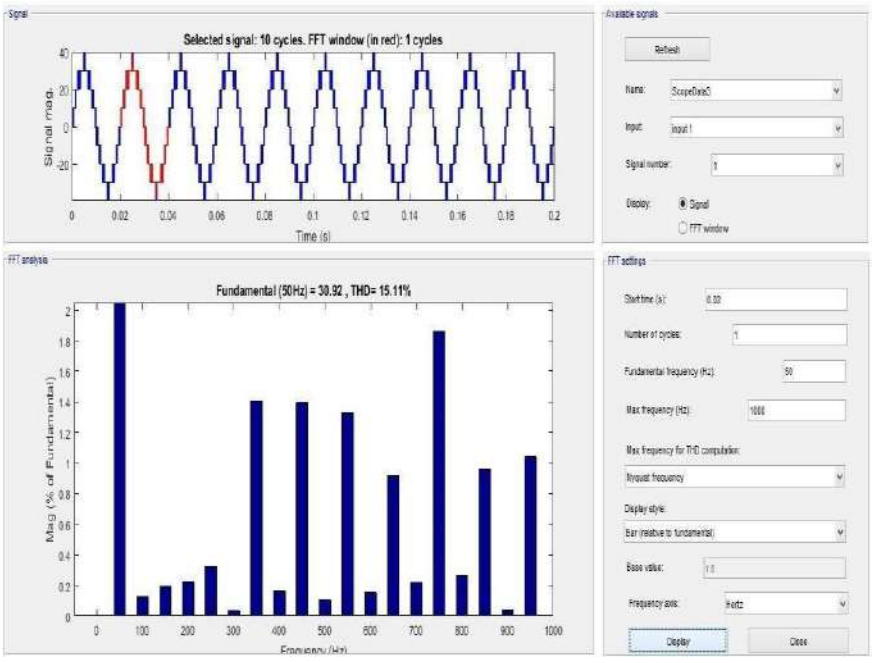


Fig 3.5: THD % of 9-level cascaded H-bridge multilevel inverter

3.6 FILTER

The line filter reduces the high frequency harmonic content of the line current caused by the switched operation of the VSI. While selection of filter cost, size and for which application it used are considered. There are different types of filters.

- L filters
- LC filters
- LCL filters

3.6.1 LC Filter

Fig 4.1 shows the structure of LC filter. In this type inductor L is in series and capacitor C is in shunt with load. The choke (L) allows the dc component to pass through easily because its dc resistance R is very small. The capacitive reactance Xc is very high for dc and it acts as open circuit. All dc current passes through across which dc output voltage isobtained.

The inductive reactance XL = 2pfL is high for ac components. Therefore the ripples are reduced. Even if any ac current passes through L, it flows through the capacitor because ofits low capacitive reactance

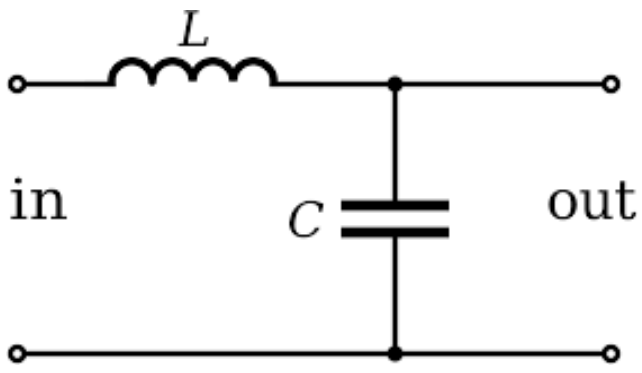


Fig 3.6: LC Filter

3.6.2 Advantages of LC Filter

Some of the advantages of LC filter are as follows

- In choke input filter, current flows continuously. Therefore the transformer issued more efficiently.
- Ripple content at the output is low.
- DC voltage drop across L is much smaller because its de resistance R is very small.
- The LC filters are useful for heavy load currents.
- It has good voltage regulation.
- LC is fine for filtering high power signals.

3.6.3 Calculation of L and C for LC filter

The inductive part of the low pass filter is designed based on the allowable current rippleat switching frequency on the grid side.

$$L = VDC / 4*f_s*\Delta i \qquad 4.1$$

Where VDC is the DC voltage, Δi value of the current ripple, f_s is switching frequency.For, calculation of capacitor,

$$C = \Delta i / 8*f_s*\Delta v0, \qquad 4.2$$

Where, Δv0 = voltage ripple. [13]

3.7 BLOCK DIAGRAM OF PROPOSED PROJECT WITH FILTER

Fig 4.2 shows the block diagram of 9-level cascaded H-bridge multilevel inverterwith filter.

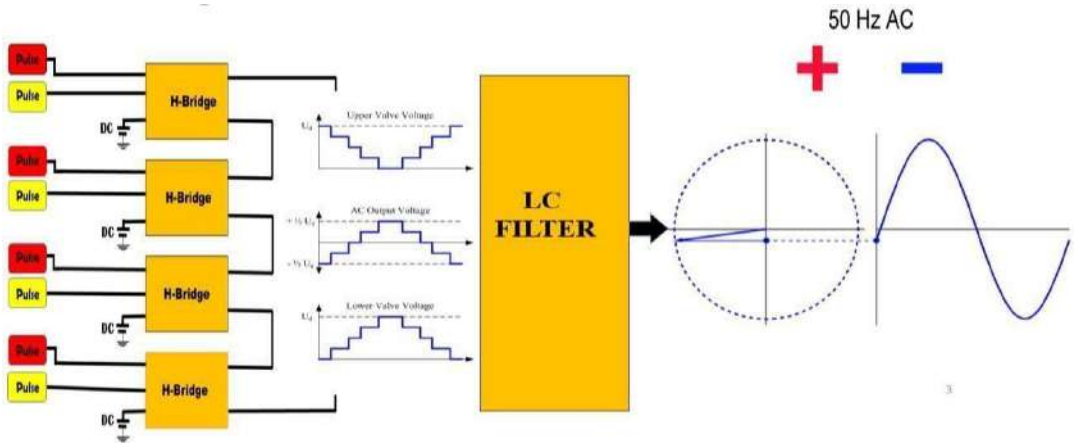


Fig 3.7: Block diagram of. 9-level cascaded H-bridge multilevel inverter with filter

3.8 SIMULATION WITH LC FILTER AND NO LOAD

Fig 4.3 shows the simulation of 9-level cascaded H-bridge multilevel inverter with LC filter. By using LC filter the THD% decreases from 15.11% to 0.37% and the output waveform is a pure sine wave.

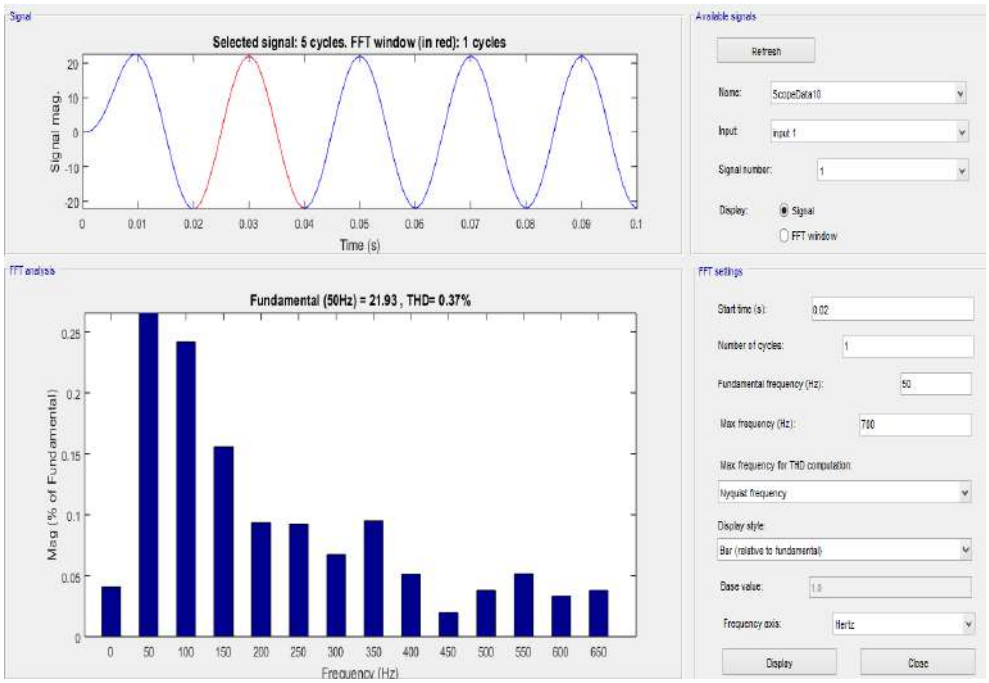


Fig 3.8: Simulation results with LC filter and No Load

3.9 SIMULATION WITH LC FILTER AND LOAD

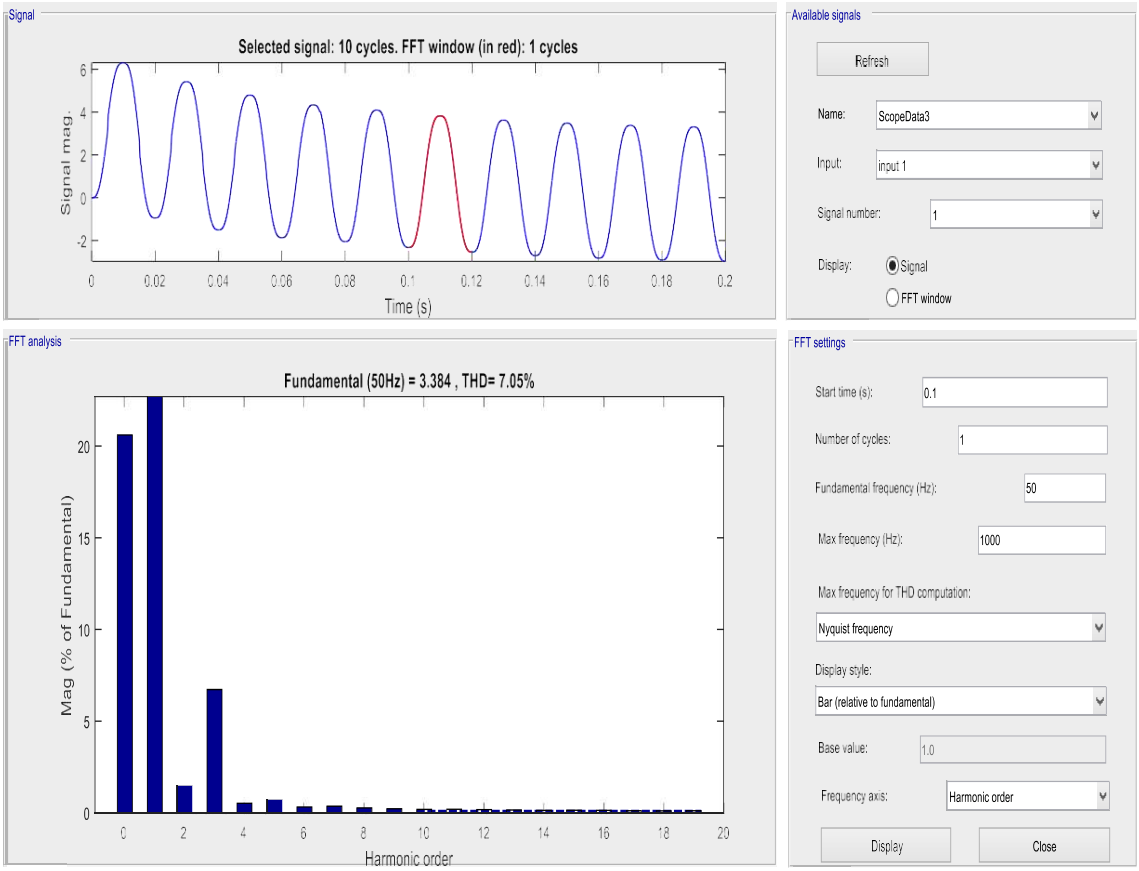


Fig 3.9: Simulation results with LC filter and Load

3.10 COMPARISON OF SIMULATION RESULTS WITH AND WITHOUT FILTER

Table 4.1 shows the comparison between the simulation results in terms of THD% of 9-level cascaded H-bridge multilevel inverter without filter and with filter.

Table 3.1: Comparison of simulation results

S.No	PWM Technique	No of Level	THD % without filter	THD % with filter & No Load	THD % with filter & Load
1.	Sine wave PWM	9 Level	15.16%	0.37%	7.05%

CHAPTER-4

COMPONENTS USED

There are various basic electrical and electronic components we have used tobuild our project circuitry, the major components are explained below.

4.1 12VOLT STEP-DOWN TRANSFORMER

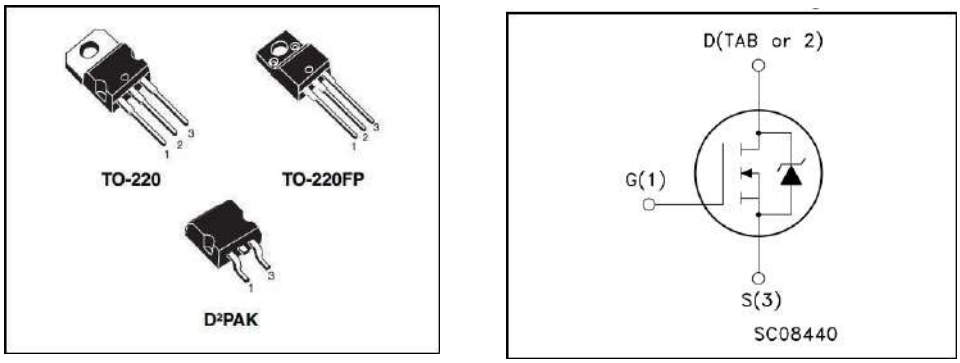
A transformer as shown in Fig 5.1,is an electrical machine which with great efficiency changes the voltage level so that the power can be transferred to very long distances without much loss. 12-0- 12V, 1A Centre-Tapped Step Down Transformer is a general-purpose chassis mounting mains transformer. Transformer has 230V primary winding and centre-tapped secondary winding. The Transformer act as a step-down transformer reducing 230VAC RMS to 12VAC RMS. It can be used in Small rectifier circuits to charge a 12V battery, Power small devices with low voltage ratings like Arduino, PIC, AVR, and Raspberry Pi and other controllers, it can also be used to charge mobile phones, etc.

Fig 4.1: 12volt Step-down Transformer

4.2 MOSFET (STP75NF75)

Fig 5.2 shows MOSFET (STP75NF75) and its internal schematic diagram. This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high efficiency, high-frequency

isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applicationswith low gate drive requirements.



(a) (b)

Fig 4.2: (a) MOSFET (STP75NF75), (b) internal schematic diagram

4.3 MOSFET DRIVER (IR2104)

Fig 4.3 shows MOSFET driver (IR2104) and its data sheet summary. The IR2104(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and lowside referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

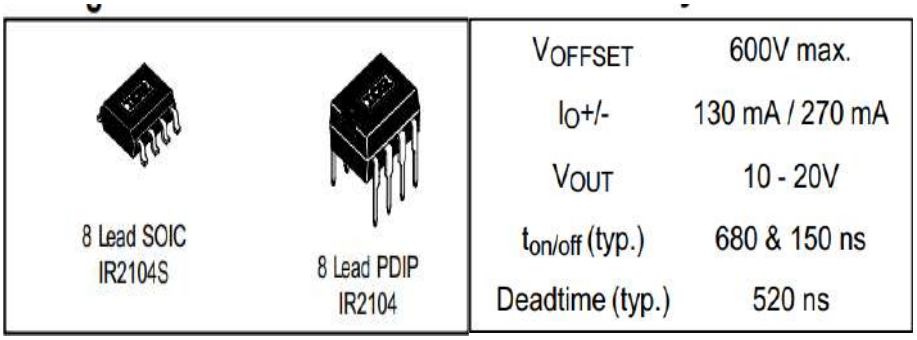


Fig 4.3: (a) MOSFET Driver (IR2104), (b) Product summary

4.4 DIODES AND RESISTORS

Fig 4.4 shows the structure of diode and resister. A diode is a specialized electronic component with two electrodes called the anode and the cathode. Diodes can be used as rectifiers, signal limiters, voltage regulators, switches, signal modulators, signal mixers, signal demodulators, and oscillators.

A resistor is a passive two-terminal electrical component that implements electrical resistance as a circuit element. In electronic circuits, resistors are used to reduce current flow, adjust signal levels, to divide voltages, bias active elements, and terminate transmission lines, among other uses.

Fig 4.4: (a) Diodes, (b) Resisters

4.5 CAPACITOR AND INDUCTOR

Fig 4.5 shows the structure of capacitor and Inductor. A capacitor is a passive electronic component that stores energy in the form of an electrostatic field. In its simplest form, a capacitor consists of two conducting plates separated by an insulating material called the dielectric. The capacitance is directly proportional to the surface areas of the plates, and is inversely proportional to the separation between the plates. Capacitance also depends on the dielectric constant of the substance separating the plates. The standard unit of capacitance is the farad, abbreviated. This is a large unit; more common units are the microfarad, abbreviated µF (1 µF $=10^{-6}$F) and the Pico farad, abbreviated pF (1 pF = 10^{-12} F).

An inductor is a passive electronic component that stores energy in the form of a magnetic field. In its simplest form, an inductor consists of a wire loop or coil. The inductance is directly proportional to the number of turns in the coil. Inductance also depends on the radius of the coil and on the type of material around which the coil is wound.

The standard unit of inductance is the henry, abbreviated H. This is a large unit. More common units are the micro henry, abbreviated μH (1 μH $=10^{-6}$H) and the milli henry, abbreviated mH (1 mH $=10^{-3}$ H).

Fig 4.5: (a) Capacitor, (b) Inductor

4.6 PC BOARD

Fig 4.6 shows the structure of PC Board. A printed circuit board (PCB) mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate. Components (e.g. capacitors, resistors or active devices) are generally soldered on the PCB.

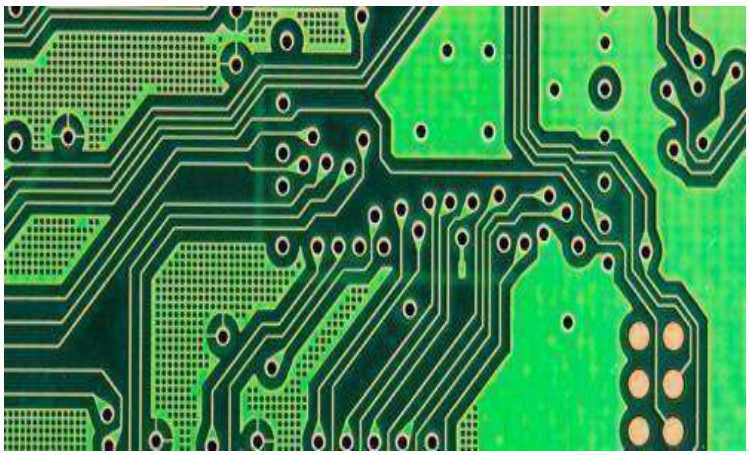


Fig 4.6: PC Board

4.7 ARDUINO NANO (AT MEGA 328P)

Fig 4.7 shows the structure of Arduino Nano. The Arduino Nano is an open-source breadboard- friendly microcontroller board based on the Microchip ATmega328P microcontroller (MCU) and developed by Arduino.cc and initially released in 2008. It offers the same connectivity and specs of the Arduino Uno board in a smaller form factor.

Nano is equipped with 30 male I/O headers, in a DIP-30-like configuration, which can be programmed using the Arduino Software integrated development environment (IDE), which is common to all Arduino boards and running both online and offline. The board can be powered through a type-B mini-USB cable or from a 9 V battery.

Fig 4.7: Arduino Nano

4.8 RESISTIVE LOAD

Fig 4.8 shows the resistive load. Resistive loads are typically used to convert current into forms of energy such as heat. Unlike inductive loads, resistive loads generate no magnetic fields. Common examples include most electrical heaters, and traditional incandescent lighting loads. As shown in Fig below.

Fig 4.8: Resistive load

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